CIRCUIT DESIGN OF A PULSE INTEGRATOR.

Sébastien VILALTE

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Laboratoire d'Annecy le Vieux de Physique des Particules
B.P. 110 74941 ANNECY-LE-VIEUX CEDEX France.
Phone : 33 4 50 09 16 00
Fax : 33 4 50 25 94 95
e-mail : vilalte@lapp.in2p3.fr

ABSTRACT:

The Pulse integrator, which is described here, is an electronic developed for the VIRGO experiment. The Pulse integrator is able to trig a pulse and to generate a ramp voltage with controlled slope and duration.

Its aim is to allow a precise time delay measurement using a slow digital acquisition. This electronic is a part of a crate, which contains a Rubidium clock.

CONTENTS: **pg.**

1- Introduction : principle and general description of the *Pulse integrator*.

The Pulse integrator allows to generate a linear ramp voltage after a positive pulse detection. The input pulse detection level voltage is **1,5V**, so the integrator is compatible with different digital and analog input signals.

The output starting level is 0V and the final level is adjustable from 0 to 10V. It is pre-adjusted to 8V.

A switch selects the integrator slope:

- ***Position 1:*** 1E5 V/s ⇔ 100µs for a 0/10V slope.
- ***Position 2:*** 5E4 V/s ⇔ 200µs for a 0/10V slope.
- ***Position 3:*** 2,5E4 V/s ⇔ 400µs for a 0/10V slope.
- ***Position 4:*** 1,25E4 V/s ⇔ 800µs for a 0/10V slope.
- ***Position 5:*** 6,25E3 V/s ⇔ 1,6ms for a 0/10V slope.
- ***Position 6:*** adjustable by trimmer from 0 to 10ms for a 0/10V slope. It is pre-adjusted to 5ms for a 10V slope.

The output offset voltage is adjustable and pre-adjusted to have the slope rupture at 0V.

The maximum input pulse frequency depends on the used slope: the pulse period has to be superior or equal to the integration duration.
A new integration is possible starting from the reset.

The slope depends only on the switch position and not on the adjustable output level.

The pulse integrator performs a constant reference voltage integration, started after an input level detection. So, It will not allow to generate any other signal than a ramp.

2- The crate:

The crate is composed of:

- 4 Pulse integrators with for each, 6 identical outputs.
  A green DEL is flashing every time the integrator detects an input pulse.

- A Rubidium clock with its outputs.

- An independent power supply, which is working on the 230VAC/50Hz mains supply.

- A fan, supplied with the +5V, to decrease the internal heating.

The 4 integrators are supplied by a linear +15V/-15V power supply.

The +5V is supplied by a switching power supply. It is common to the 4 integrators and the Rubidium clock.
The use of a switching power supply is needed because of the clock consumption: warm-up 17W; operating 15W.

Available Rubidium clock outputs:

- 1PPS output: 0-5V pulse (ACMOS).
  Pulse duration 400ns.
  Jitter < 10ps RMS.
  Time to lock: 5 min.
  Accuracy at lock: 5E-8.
  Accuracy <1E-9 after 7,5min.

  A green DEL is flashing at every pulse.

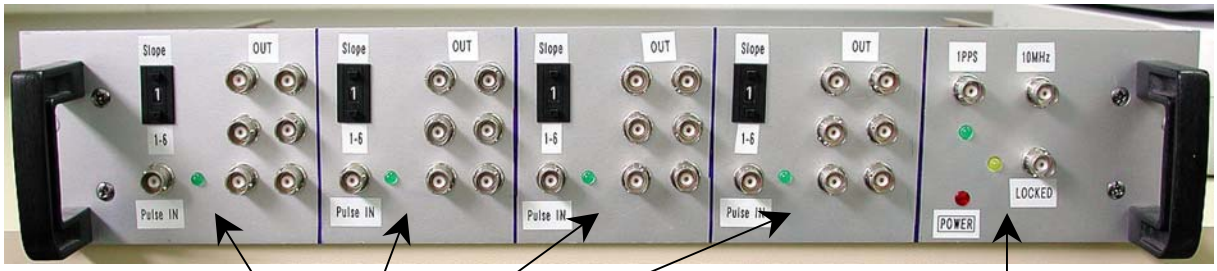
- 10MHz reference output: 7,8dBm (≈0,8Vpk/50Ω).

- Lock output: 0-5V TTL/CMOS compatible.
  The lock signal is high when the clock is locked (accuracy=5E-8).

  When the clock is locked, a yellow DEL is light on.

- A red DEL indicates the power is ON.

Front view of the crate:



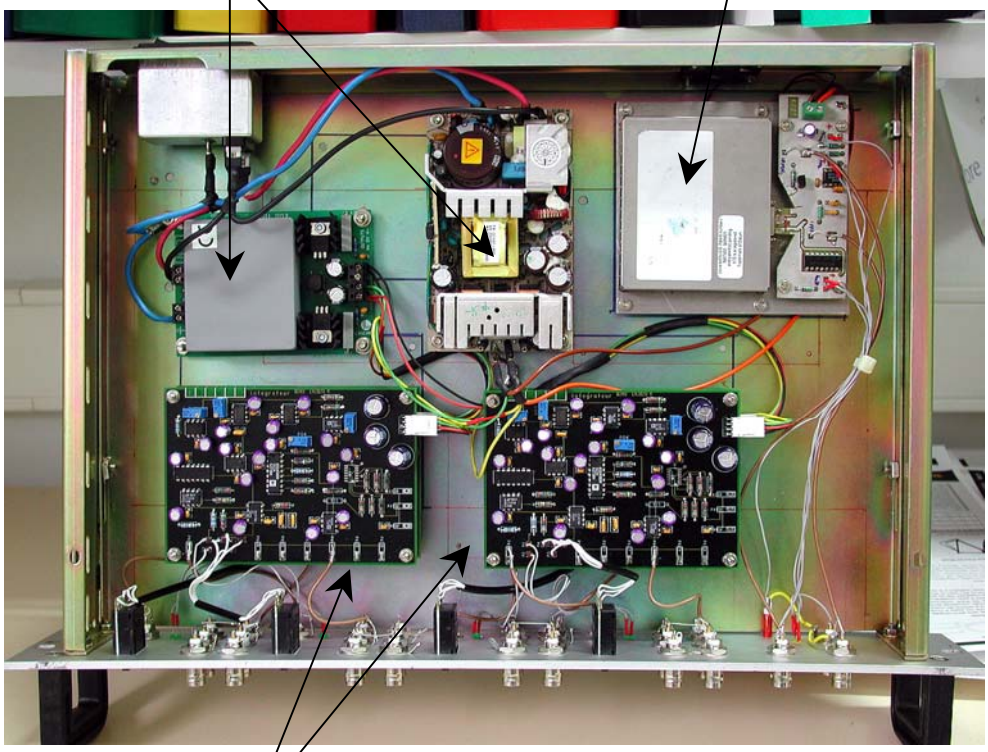
4 Pulse integrators

Rubidium clock

Inside view of the crate:

Power supplies

Rubidium clock



Integrators

3- *Pulse integrator* technical description and solutions.

The electronic has to generate a linear ramp trigged on a short pulse.
The ramp duration has to be a constant time.

The chosen technical solution is to integrate a reference voltage using a switched capacitor and several switched resistors, to change the output signal slope.

An adjustable output level detection resets the integrator.

3-1 The pulse integration principle :

(cf. following simplified integrator schematic)

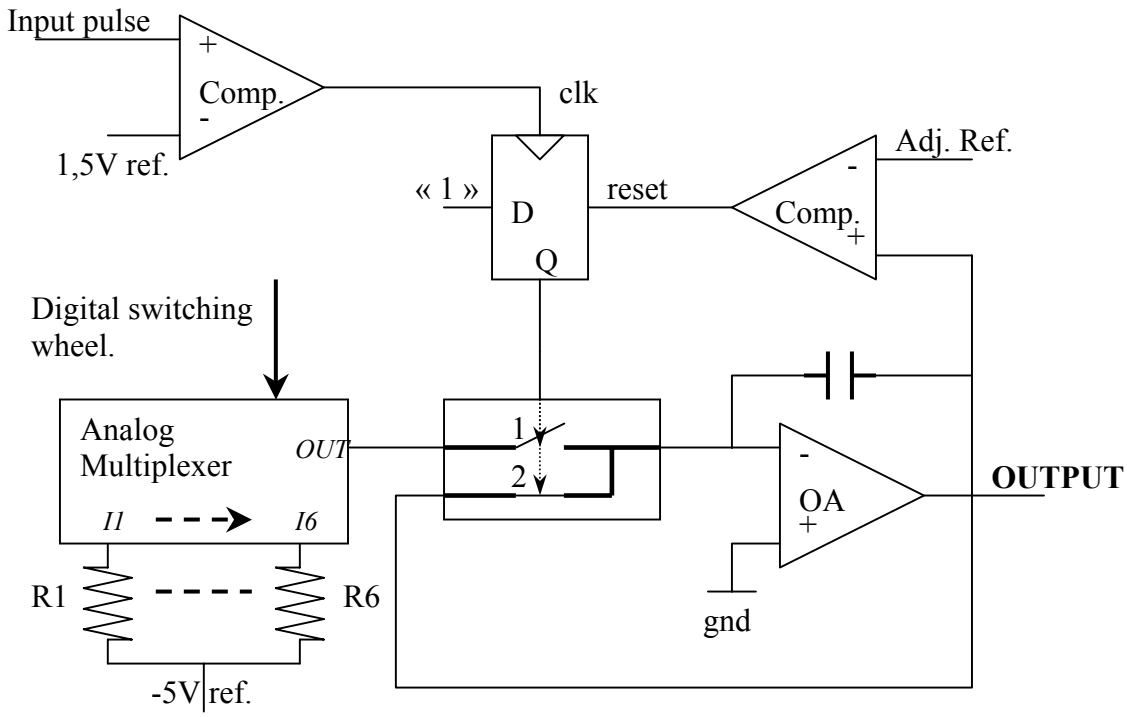
- Fast input pulse detection:
  A fast comparator detects an input voltage level superior to 1,5V.
  Its positive output starts the integration.
  Its negative output is used to perform the flashing DEL, using a monostable component.

- The positive comparator output commands a flip-flop gate clock, which allows to have a memory of the pulse, even its is very short. The transmitted data (D) to the output (Q) is a digital high level ("1").

- The flip-flop output drives a double analog switch.
  It allows to begin the integration. When switch1 is ON, switch2 is OFF.
  So, before the pulse detection, Q is low, switch1 is OFF, switch2 is ON; the integrator is working as a ground follower.
  When a pulse is detected, Q turns high, switch1 is ON, switch2 is OFF: the operational amplifier is working as an integrator.

- A second comparator, with an adjusted voltage level, resets the flip-flop. So, the two switches turn and the capacitor is discharged. The integrator is reset.

- A digital switch selects the integrator slope using an analog multiplexer.



Simplified integrator schematic

All the reference voltages are adjustable.

The important point is to have a very stable –5V reference to have good integrator linearity: this voltage is performed using a voltage reference component.

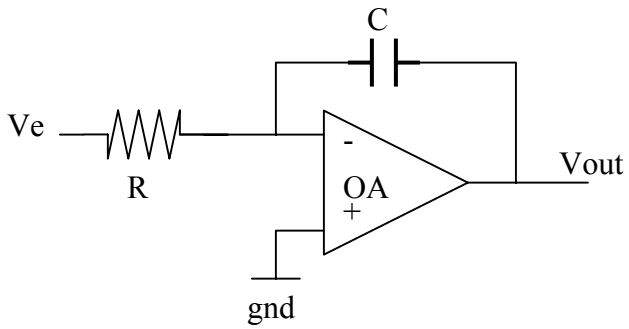
The advantage of this solution is to have a linear slope, a very low offset output voltage adjustable using a trimmer and a ramp independent from the input pulse.

An output buffer drives the 6 final outputs.

The 1st advantage of the slope digital control is to keep all the analog signals on the printed board. The 2nd advantage is to be compatible with an external 3bits decimal digital code.

3-2 The integrator :

The linear ramp is performed using an operational amplifier as an integrator. Here, we integrate a constant –5V voltage reference:



$$Vout = \frac{-1}{RC}\int Ve(t)dt$$

If Ve is a constant voltage ***Vref*** (here,-5V),
we will obtain:

$$Vout = \frac{-1}{RC} Vref.t$$

Vout=Vref if t=RC.

Multiplexing different values for R, we can have different slopes.
A reset of the integrator is needed to re-start the output to 0V.

The switches used to reset the integrator have a ≈20Ω resistance.

When the integration has started, Switch2 is OFF, so its resistance is infinite. It assures the linearity of the output signal ramp, because this switch is in parallel with the capacitor. Switch1 is ON.

If the slope has to be well known, it will have to be calibrated; because of the resistances and capacitance accuracies.

3-3 Output offset :

The switched capacitor system allows to have a more linear response than a resistor feedback system (feedback capacitor and resistor).

The disadvantage of this system is the stocked charge in the double switch: until a pulse is detected the switch1 is OFF and switch2 is ON. When the integration starts, the charge stocked in switch1 is transferred in the feedback capacitor and create an output offset.

To reduce this phenomenon, we had to increase the capacitance.
To obtain the same slopes, if we increase the capacitance, we have to decrease the resistances. So, as the current we can apply to the multiplexer limits us, resistances must have minimum values.

This phenomenon is visible particularly for the low slopes but the output offset voltage is the same for all the slopes.

The output offset voltage is adjusted to start the slope at 0V (see the tests part).

Remark:

In a feedback capacitor and resistor system, the feedback resistor is in parallel with the capacitor and discharges the capacitor after the integration. This resistor reduces the linearity. When the resistance increases, the linearity increases but the delay to reset increases.
In this case, the output offset voltage is hard to adjust because of the high negative gain amplifier made with the input resistor and the feedback resistor.

4- Adjustments.

(cf. schematic & board implantation)

The pulse integrator is working with different reference voltages. These voltages can be adjusted to have a more accurate output signal or for specific applications.

- The slopes depend on the capacitor and resistor values.
  These slopes will not be exactly as foreseen because of the accuracy of the components.
  The slopes depend also on the integrated reference voltage.
  It is pre-adjusted to –5V.
  For a specific application where the slope should be controlled, the reference voltage could be adjusted using the trimmer **PO2**.

- The output level when the integrator is reset can be adjusted from 0 to 10V using the trimmer **PO1**.
  It is pre-adjusted to 8V.

- The slope #6 can be adjusted using the trimmer **PO4**.
  It is pre-adjusted to a 4ms slope for an 8V output voltage excursion.

- The output offset can be adjusted using the trimmer **PO3**.
  It is pre-adjusted to –11mV to have the slope rupture at 0V.

5- Test results.

5-1 Functionalities:

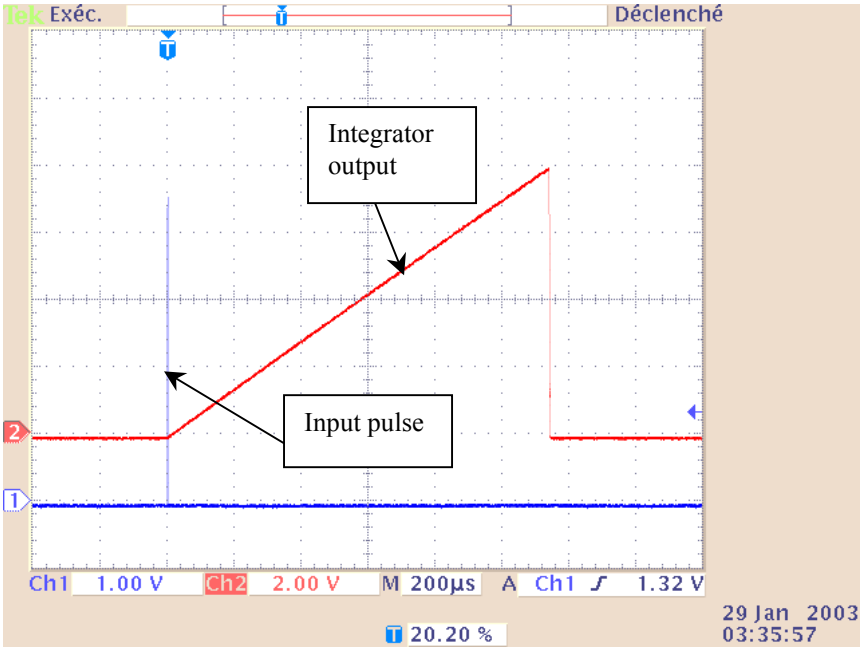
The 4 integrators are supplied by a linear +15V/-15V power supply.

The power supply consumption is **300mW** for one integrator.
So, the total electronic consumption for the linear supply is about **1,2W** (with an high impedance load).

5-2 Integrated output:

- ***Typical integration output:***

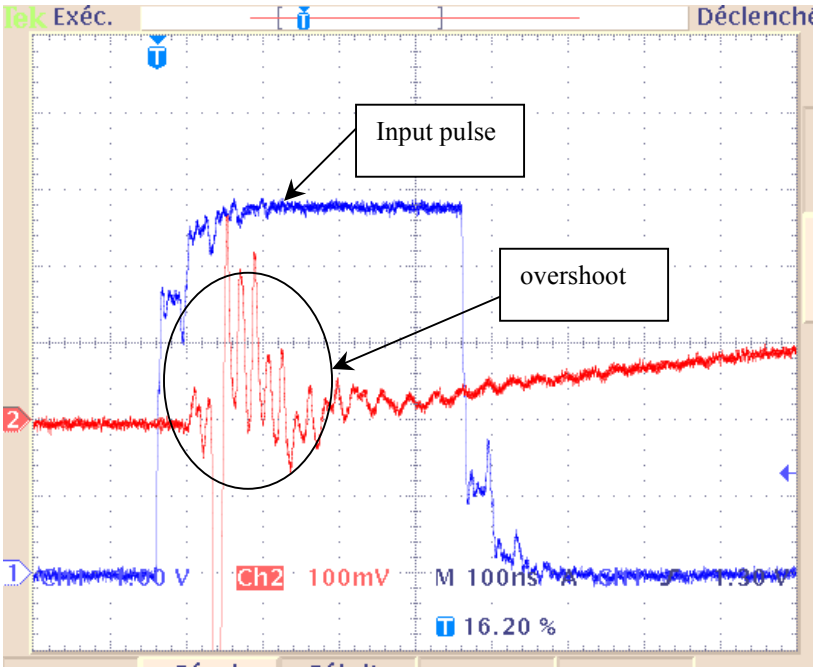
The following curve is typical 400ns Rubidium clock pulse integration. The slope position is #5, so for a 0V to 8V ramp, the theoretical integration time is 1,28ms. It is the observed slope. All the slope selections have been checked with good results.



- ***Pulse to integration delay:***

The integration starts from 50ns to 80ns after the pulse detection. This delay will depend on the integrator but will be a constant.

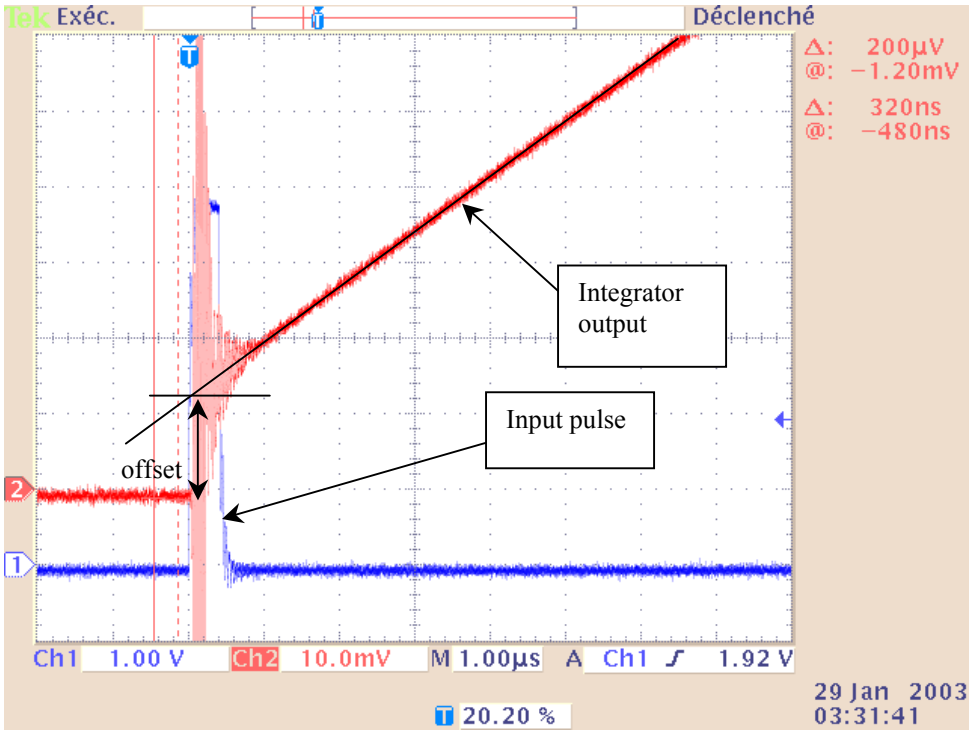
At the beginning of the integration, we can see an overshoot on the signal. This overshoot is about ***300mV*** and very quick: about ***100ns***.
It is not a problem for the slope because it is centered on the linear signal.



This overshoot is due to the switching of the capacitor and cannot be easily prevented but it will be not a problem regarding to the sample frequency (20kHz).

- ***Output offset voltage:***

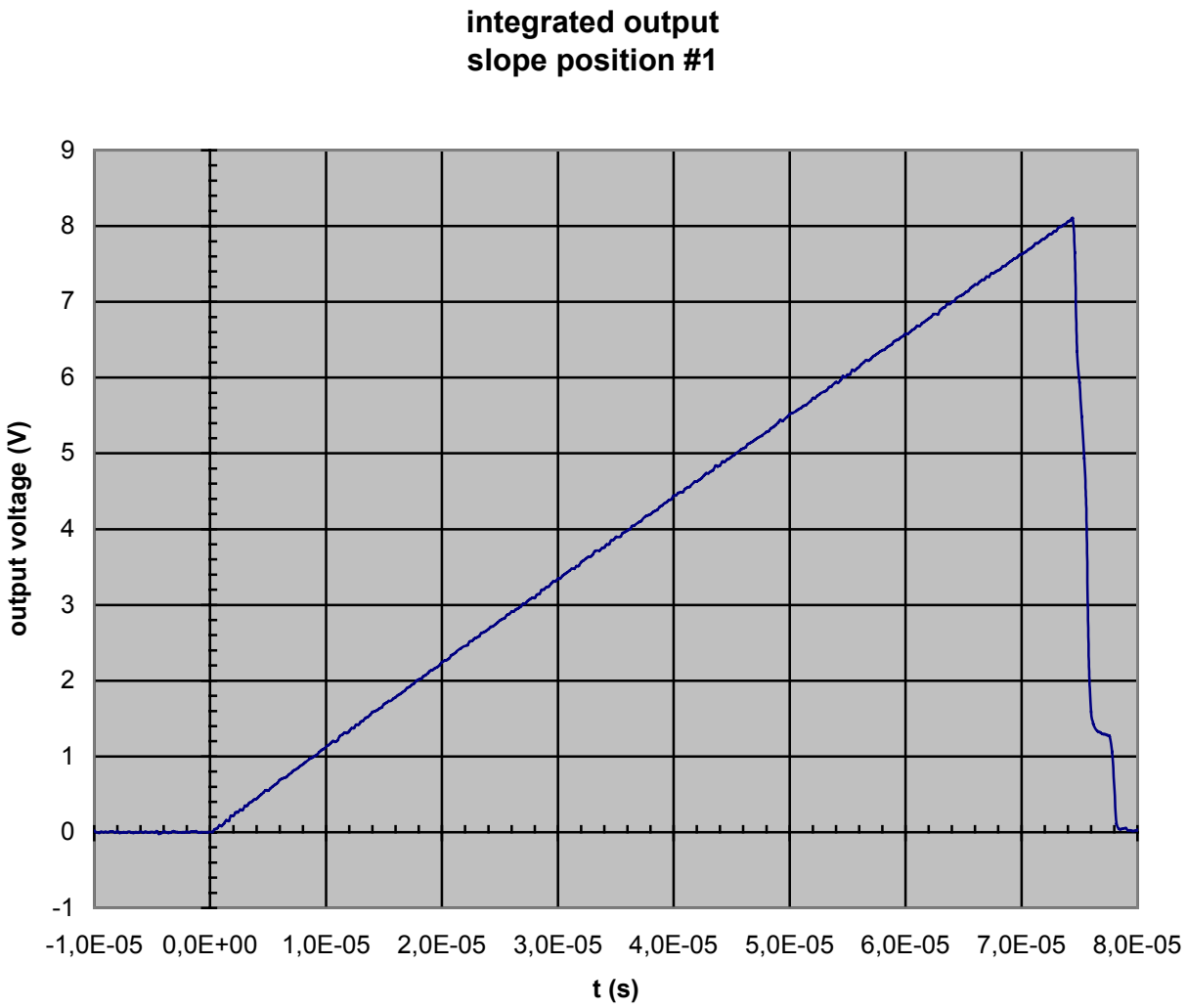
The following curves show a slope #5 position integration before adjustment.
The phenomenon is visible especially for very low slopes but is the same for all the positions.
This offset is adjusted to have the beginning of the ramp at 0V.



This adjustment is important for absolute delay measurement.

- ***Output linearity:***

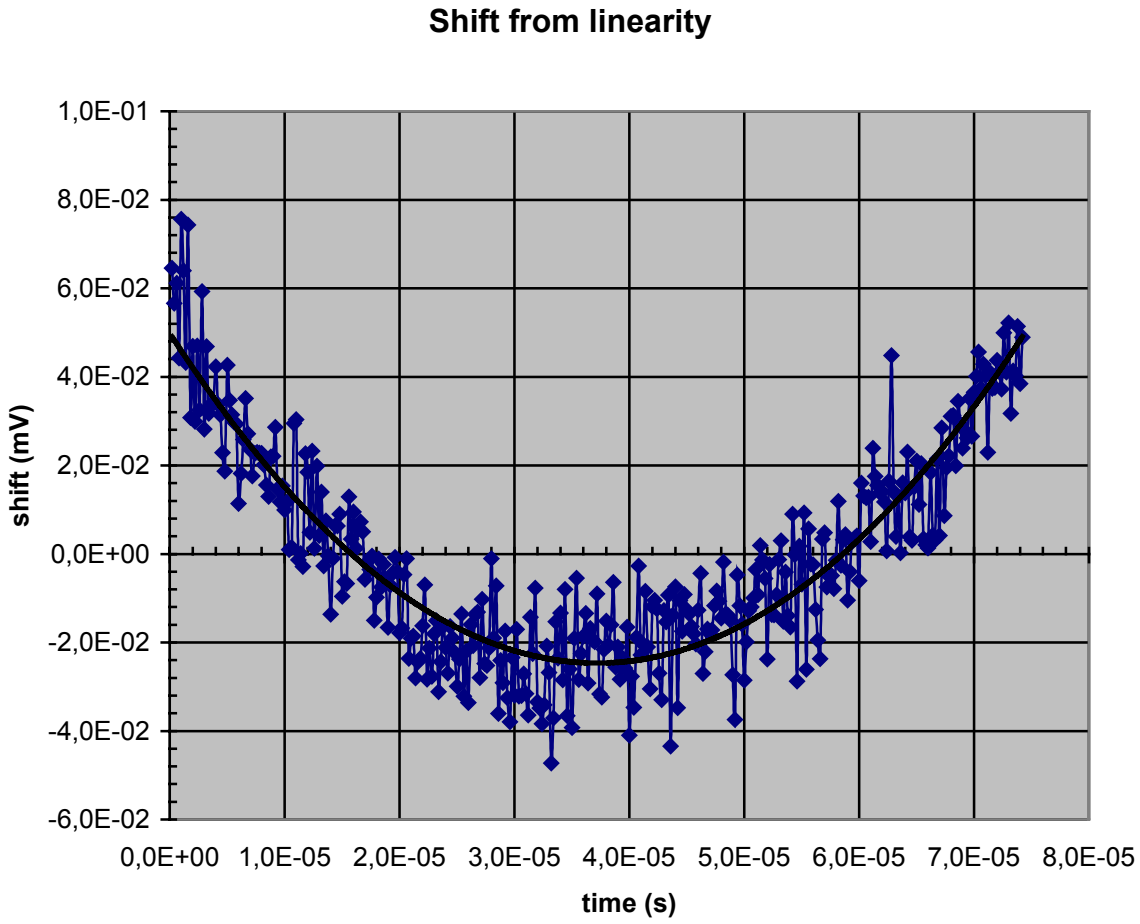
The following curve is obtained with digital oscilloscope data.



The time basis is centered on the oscilloscope trigger (0 second).

We can see the integrator is reset for an ≈8V output voltage.

If we fit the ramp with a line and process the data, we can see the shift from linearity in the following curve:



We can see the shift is about 60mV on an 8V range which is corresponding to a **0,75%** shift from linearity on the range.

When we fit the shift, we can see it is a parabola.
In the future applications, this non-linearity should be compensated for more accuracy by processing the data.

6- Conclusions.

This pulse integrator will allow to perform a linear ramp triggered on a positive pulse with a shift from linearity about 0,75% on its full range. For more accuracy, the data can be processed.

The slopes can be selected from 6,25E3 V/s to 1E5 V/s.

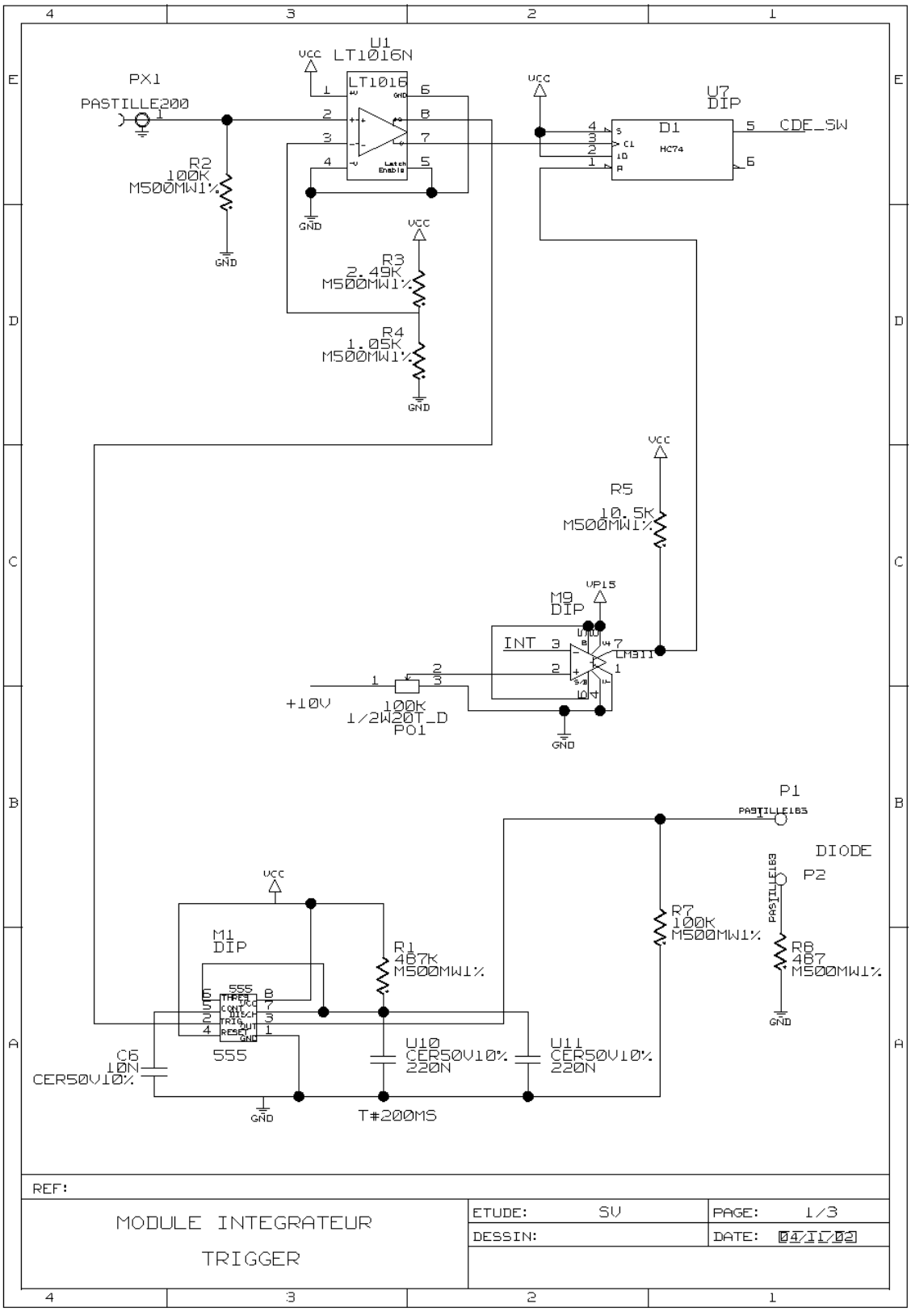
It will be typically used to measure accurately relative time delays.

It is compatible with different input pulse levels and durations.

The system is compatible with differential transmission lines: it has been designed with a second differential output.

APPENDIX :

SCHEMATICS – BOARD IMPLANTATION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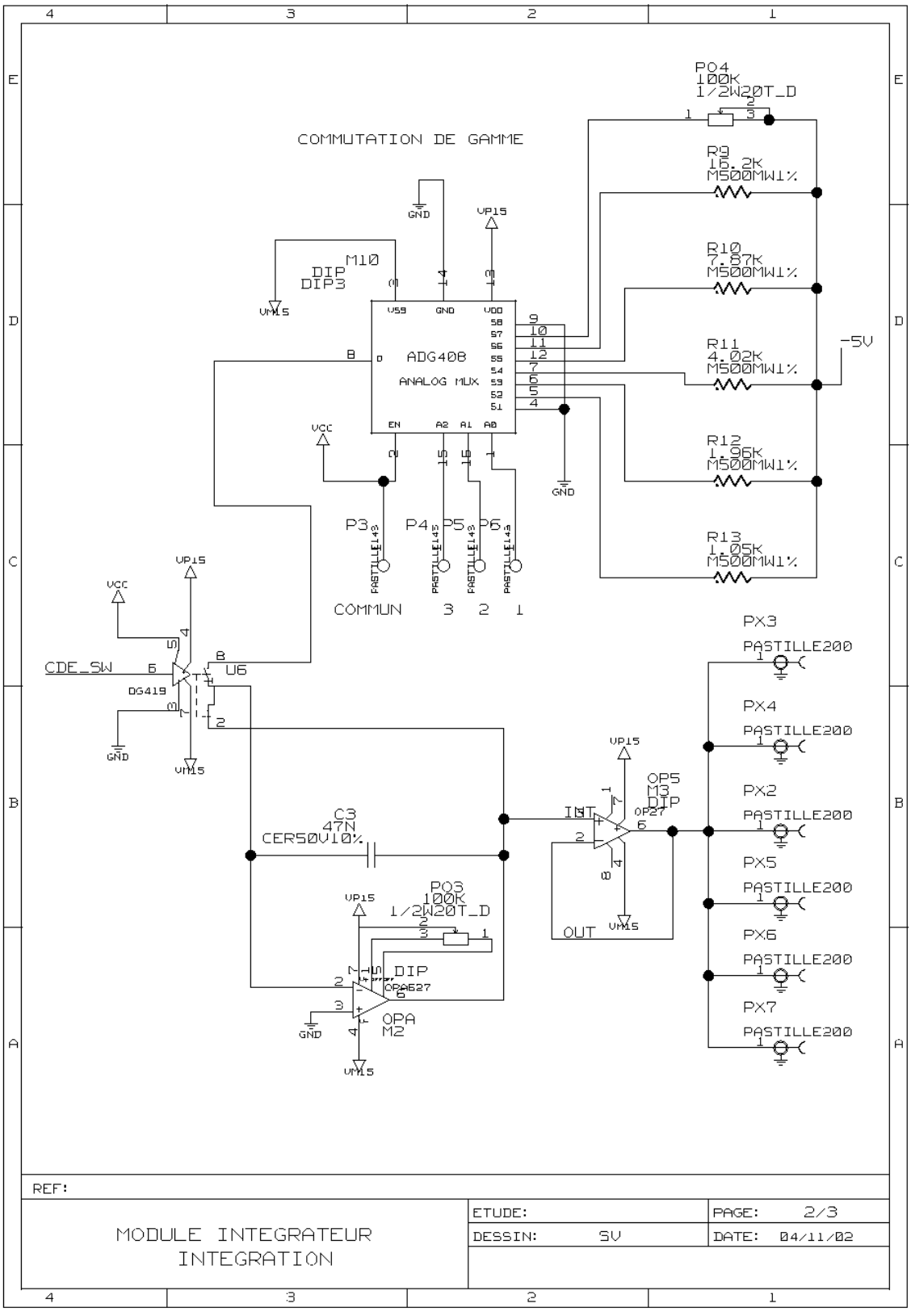
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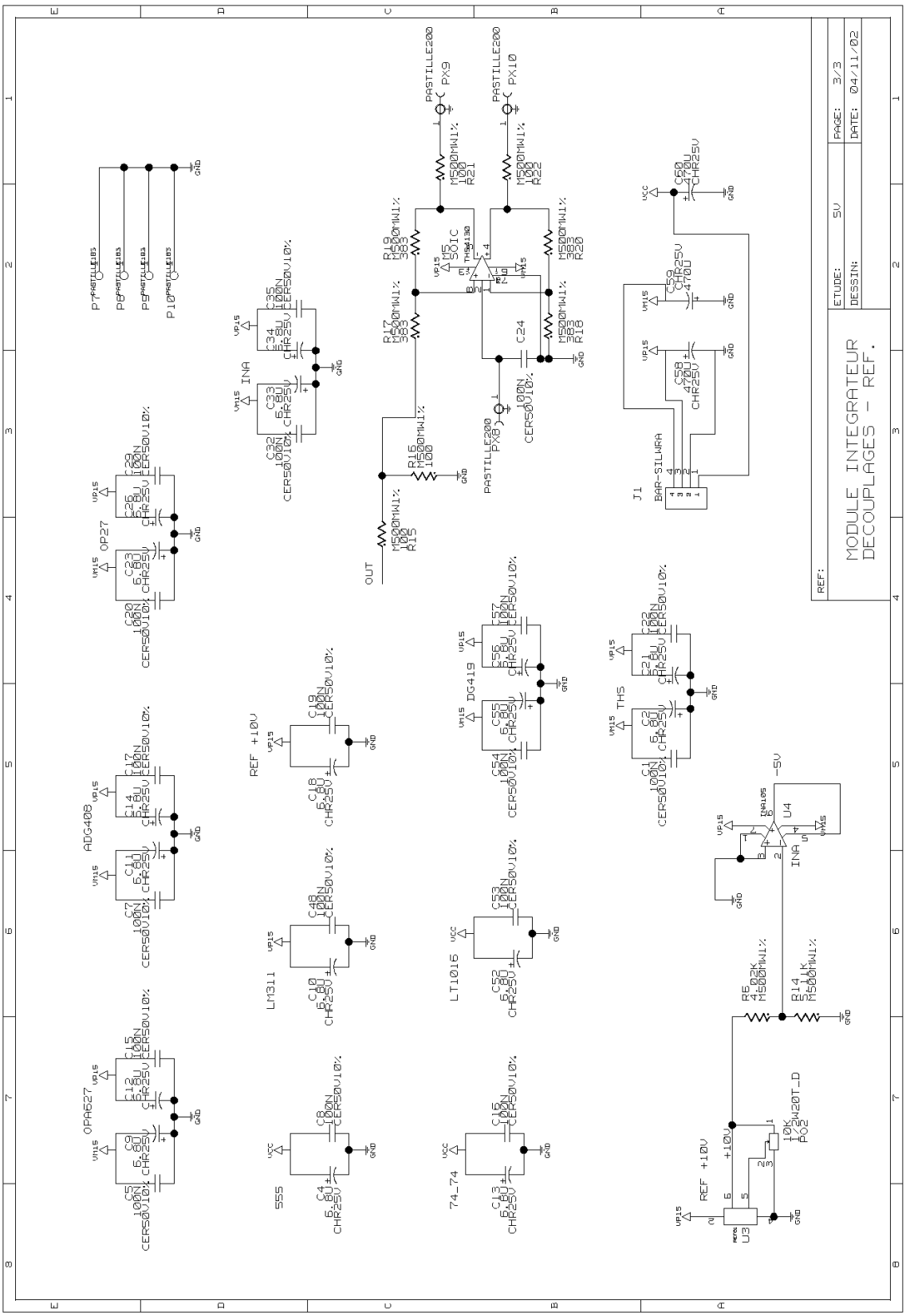
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BOARD IMPLANTATION