**Istituto Nazionale di Fisica Nucleare**
*Sezione di Pisa*
Largo Bruno Pontecorvo, 56127 Pisa – Italy
http://www.pi.infn.it

**VIRGO Collaboration**

# UDSPT Board Output Noise

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# 1. INTRODUCTION

## 1.1 *Document Purpose and Scope*

This document was written to provide an overview of UDSPT board output stage configuration and associated noise. The UDSPT board ([RD1]) is a high performance signal conditioning, signal conversion and processing platform. Boards, developed within the scope of the Advanced VIRGO SAT sub-system for the control of Superattenuators, are equipped with 6 x 24bit channels ADC and 6 x 24bit channels Digital to Analog Converter (DAC).

A brief description of output stage together with some measurements and SPICE ([RD3]) simulations of DAC and output stage is presented in this document.

## 1.2 *Reference Documents*

**[RD1]** Gennai et al., The New High Performance Suspension Control System for Advanced VIRGO, VIR-0374A-15, September 2015

**[RD2]** Analog Device, AD1955 Datasheet (http:/www.analog.com/media/en/technical-documentation/data-sheets/AD1955.pdf)

**[RD3]** Nagel, L. W, and Pederson, D. O., SPICE (Simulation Program with Integrated Circuit Emphasis), Memorandum No. ERL-M382, University of California, Berkeley, Apr. 1973

**[RD4]** R.M. Dolby, An Audio Noise Reduction System. Journal of the Audio Engineering Society, October 1967

**[RD5]** http://www.ti.com/lit/ds/symlink/opa544.pdf

**[RD6]** http://www.analog.com/media/en/technical-documentation/data-sheets/AD8397.pdf

**[RD7]** http://www.ti.com/lit/ds/symlink/opa1612.pdf

## 1.3 *Acronyms*

| | |
|---|---|
| ***ADC*** | Analog to Digital Converter |
| ***DAC*** | Digital to Analog Converter |
| ***DSP*** | Digital Signal Processor |
| ***OPAMP*** | Operational Amplifier |
| ***PCB*** | Printed Circuit Board |
| ***RD*** | Reference Document |
| ***SNR*** | Signal To Noise Ratio |
| ***SPICE*** | Simulation Program with Integrated Circuit Emphasis |
| ***UDSPT*** | Boards developed for Advanced Virgo SAT control |

# 2. UDSPT BOARD

## 2.1 *Introduction*

The UDSPT board is a high performance signal conditioning, signal conversion and processing platform that enables users to implement state-of-the-art hard real-time control system. Board can be operated in standalone mode or in cooperation with other UDSPT boards. Board was developed within the scope of the Advanced Virgo Project aimed to direct detection of gravitational waves and founded by Italian INFN and French CNRS. The UDSPT form factor is a variation of a Double Compact Module PICMG® AMC.0 R2.0 AdvancedMC module (variation consists in a wider board than what specified for a Double Module).

The key features of the UDSPT board include:

- Texas Instruments' multi-core DSP – TMS320C6678
- 512 Mbytes of DDR3-1333 Memory
- 64 Mbytes of NAND Flash and 16MB SPI NOR Flash Memory
- Two Gigabit Ethernet ports supporting 10/100/1000 Mbps data-rate – one on AMC connector and one front RJ-45 connector
- 170 pin B+ style AMC Interface containing Serial RapidIO (SRIO) and Gigabit Ethernet
- IRIG-B input
- Module Management Controller (MMC) for Intelligent Platform Management Interface (IPMI)
- Two on board FPGA: one Xilinx Spartan3 one Altera Cyclone IV
- 6 x 24b 3.84 MHz ADC converters
- 3 x 24b 320 kHz DAC stereo converters (6 channels individually addressable)
- Converters sampling frequency DSP IRQs synchronous with IRIG-B signal
- Fully differential input channels and balanced output channels

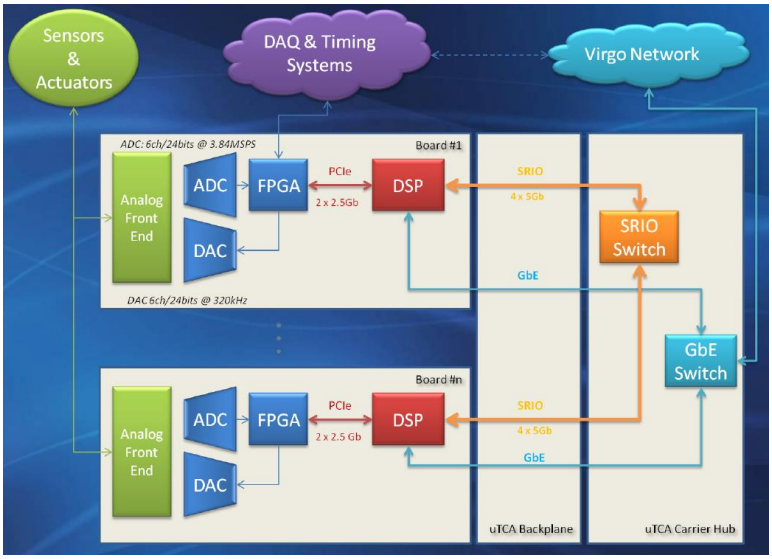


**Figure 1. UDSPT board block diagram and interfaces**


**Figure 2. Customized MicroTCA chassis hosting 12 UDSPT boards**

## 2.2 *Digital to Analog Converter*

UDSPT board host three Analog Devices AD1955 ([RD2]) stereo DAC system for a total of 6 channel individually addressable.

The AD1955 is a complete, high performance, single-chip, stereo digital audio playback system. It is comprised of a multibit sigma-delta modulator, high performance digital interpolation filters, and continuous-time differential current output DACs. The AD1955 is fully compatible with all known DVD audio formats including 192 kHz as well as 96 kHz sample frequencies and 24 bits. In UDSPT board DAC channels are used with 320 kHz sample frequency.

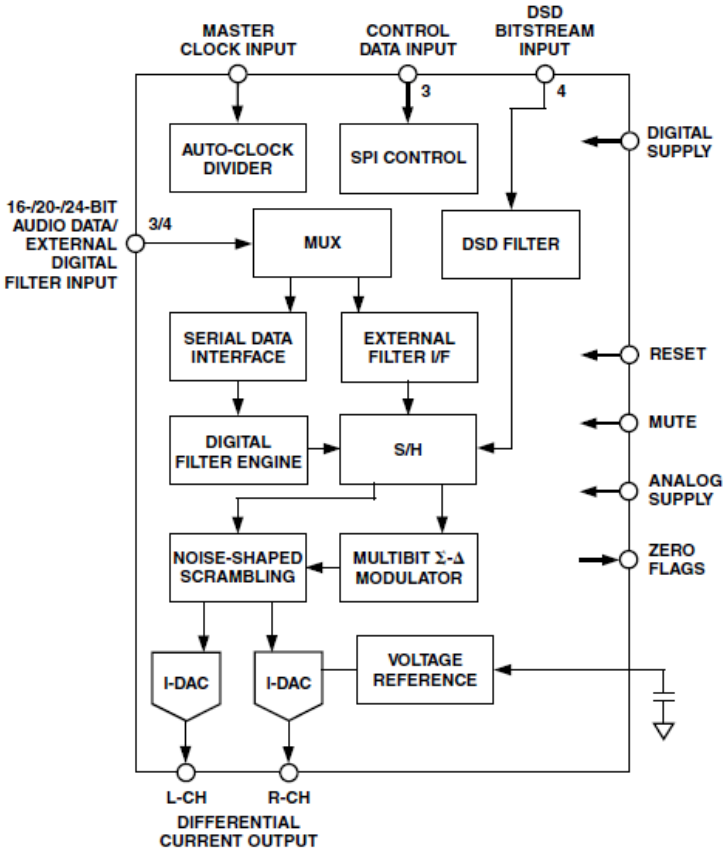


**Figure 3. AD1955 Functional block diagram**

## 2.3 *Output Stage*

### 2.3.1 Overview

UDSPT Output stage can be sketched as follows:

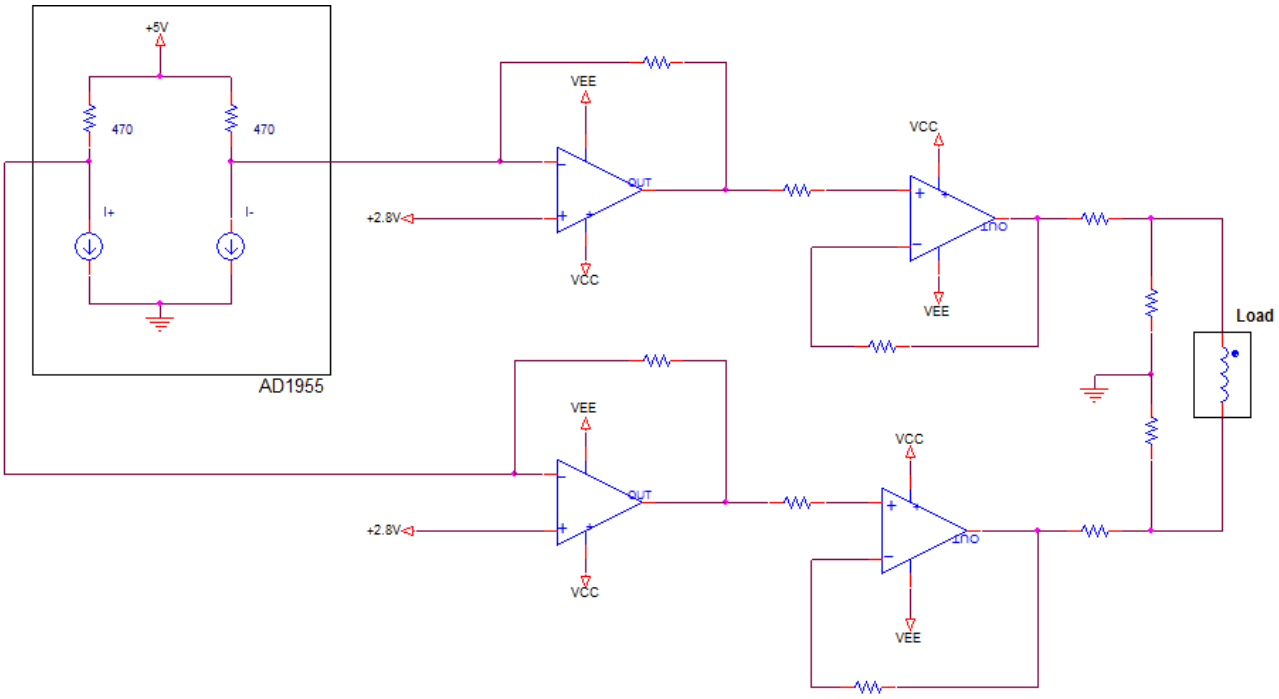


**Figure 4. Simplified output stage**

DAC output currents are converted into a differential voltage by a low noise transimpedance stage whose output is then fed to the final stage that provides required current to load (often inductive in VIRGO). Output is balanced and maximum voltage swing is 20 Volts peak-to-peak.

### 2.3.2 Configurations

UDSPT board output stage can be configured as balanced (20 $V_{pp}$ voltage swing) or as single ended (10 $V_{pp}$ voltage swing). Output resistance value can be adjusted to match specific application ranging from 0 up to few 100 $k\Omega$.

### 2.3.3 Output Current

Depending on peak output current required, a different output OPAMP could be installed (version P4 and P6 share the same PCB):

- 2 A (version P5): Texas Instruments OPA544 ([RD5])
- 310 mA (version P4): Analog Devices AD8397 ([RD6])
- 40 mA (version P6): Texas Instruments OPA1612 ([RD7])

### 2.3.4 Noise Shaping

When signal to be converted by the DAC has a coloured spectrum, dominated for example by low frequency components, we can try to increase total SNR using a digital emphasis filter before sending data to the DAC. Filter is then compensated by an analog de-emphasis filter. Whitening signal before conversion allows using the full DAC dynamics on all operational frequency range. In fact, when digital signal to be converted has a non-white spectrum, signal can be digitally amplified in frequency region where it is smaller. If signal is dominated by low frequency part, signal can be amplified at high frequency without reducing the total dynamical range. This well-known technique (see for example Dolby A, [RD4]) allows a signal compression that usually ranges between 10 and 20 dB. In order to have a constant overall frequency response, signal must be then uncompressed by analog filters after digital to analog conversion.

Compression is in general limited by allowable reduction of dynamical range and moreover by noise of analog filters and noise of final stages. Other limitations come from poorer performances in terms of total harmonic distortion (and therefore noise up-conversion) due to high value capacitors inserted in signal path and poorer electromagnetic noise immunity, both suggesting limiting compression to the minimum.

UDSPT boards can be equipped with a first or second order de-emphasis filter with a cut-off frequency that can be set down to the 1 to 10 Hz region.

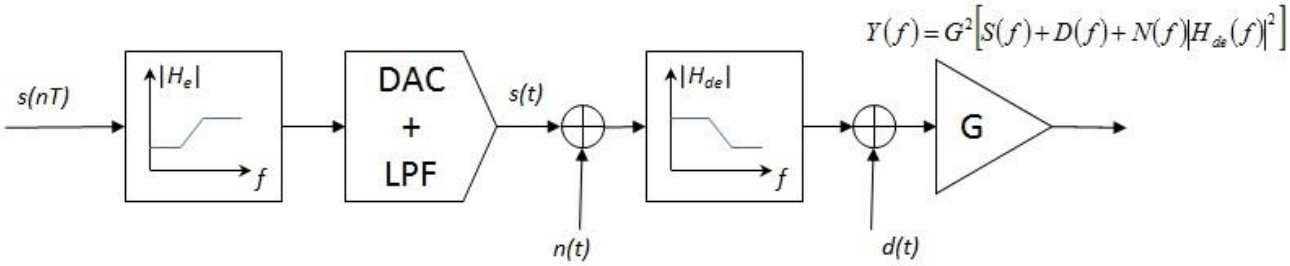


**Figure 5. Noise shaping. If the signal *s(t)* to be converted has a coloured spectrum and if the dominating noise is *n(t)*, applying a digital emphasis filter $H_e(f)$ followed by an analog de-emphasis filter $H_{de}(f)$ such that $H_e(f)H_{de}(f)=1$, signal to noise ratio at the output is improved**

## 2.4 *Noise Measurements and Simulations*

### 2.4.1 Measurements

Digital to analog converter noise was measured using one P4 board. The two black lines in the following plot represent a simplified noise model. The second plot shows DAC and output stage behaviour when converting a low frequency signal.

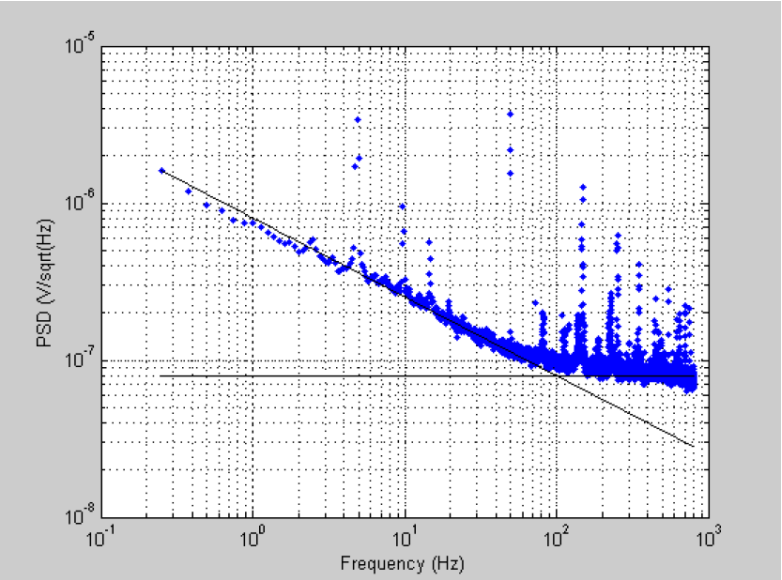


**Figure 6. Measurement of DAC noise (P4 configuration) when converting zero signal. The lines are a simplified noise model: 0.8e-6/sqrt(f) V/sqrt(Hz) at low frequency and 80 nV/sqrt(Hz) above 100 Hz. Plots includes contribution from output stage and actual DAC noise can be estimated to be slightly below the black line (i.e. about 75 nV/sqrt(Hz) at high frequency)**

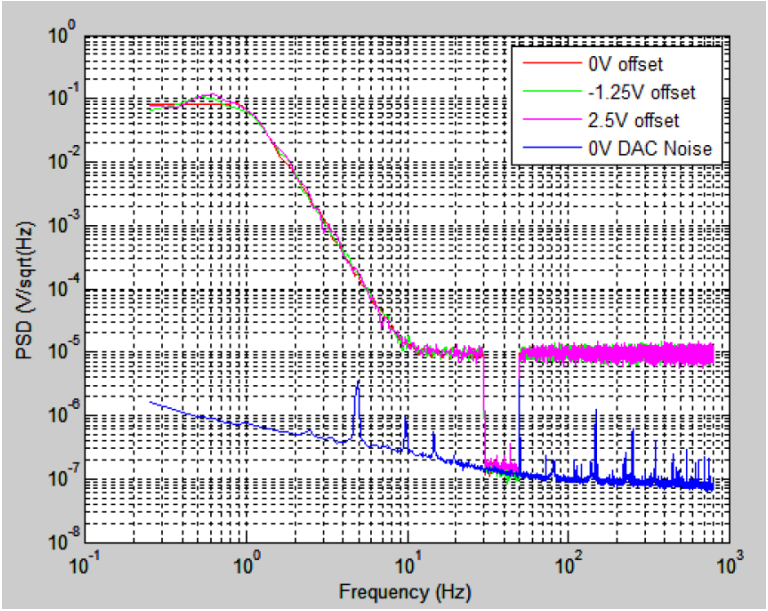


**Figure 7. DAC output spectrum when converting white noise filtered low pass (4 poles @ 1Hz + 4 zeroes @ 10 Hz) and stopband (30-50 Hz, Bessel 12th order,0.1dB ripple, -60 dB stopband). Signal amplitude was set to 0.6Vpp. To be noticed the almost negligible change in noise level compared to the 0V case.**

## 2.4.2 Simulations

SPICE simulations where made to evaluate effect of de-emphasis filters together with change of final stage OPAMP. Few significant cases are reported in following plots. To be noticed that simulation did not include actual load and that noise is evaluated at output of final stage OPAMPs (i.e. zero Ohm output resistance and no load applied). Estimated error on simulations output is in the 10 to 20% range due to uncertainties in OPAMP SPICE models behaviour at low frequency where $1/f$ noises are dominant.

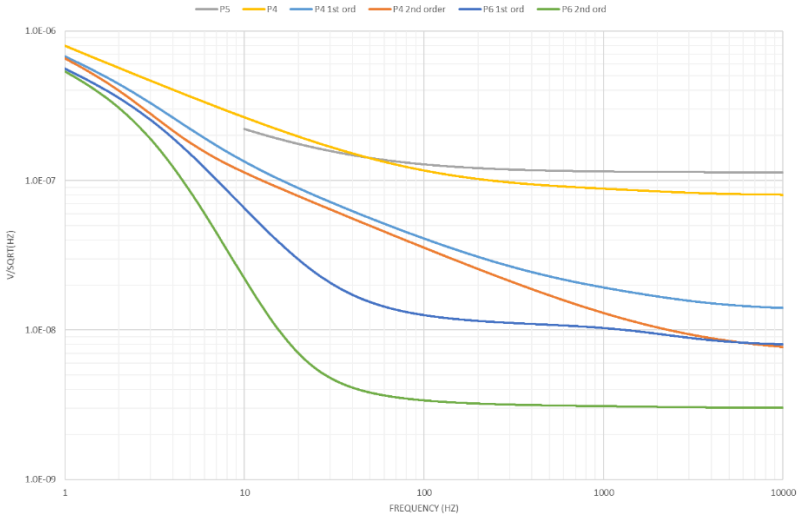


**Figure 8. SPICE simulation of total output noise for different configurations (not all cases reported). Simulations did not include output series resistor contribution. Where used, shaping filters poles were set at 3 Hz and zeros at 30 Hz. P5 contribution is underestimated since based on voltage noise only and without 1/*f* part**

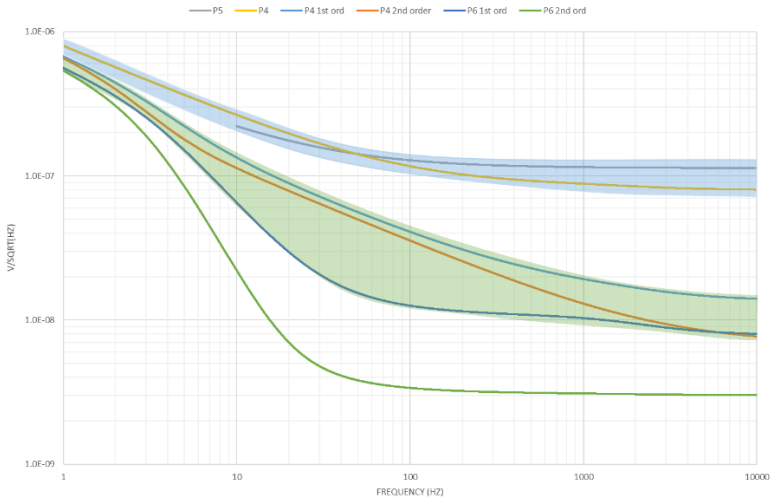


**Figure 9. From SPICE simulation we can clearly identify 2 distinct zones. The upper zone shows the behaviour without any signal compression, with high frequency noise in the 80 to 120 nV/sqrt(Hz) range. The green zone shows behaviour with 15 to 20 dB signal compression obtained with a first order shaping filter. The green line at bottom shows simulated output with a 40 dB signal compression (2nd order shaping filter): in this case it evident how output stage noise limits noise reduction to about 28 dB with a consequent reduction of spectral dynamical range**

# 3. CONCLUSIONS

SPICE simulations show that reducing output current requirements could improve noise performances. In particular, reducing peak current below 40 mA would allow some gain in the 10-100Hz range. Use of noise shaping would produce benefits in terms of signal to noise ratio with signal compression up to about a factor 20-25.

It is important reminding that simulation did not include actual load and that noise is evaluated at output of final stage OPAMPs (i.e. zero Ohm output resistance and no load applied). P6 version has a final stage that produces about 3nV/sqrt(Hz) of noise voltage at the output, equivalent to 600Ω of resistive load. In other words, benefits produced by a lower noise amplifier are effective only is real part of load impedance is smaller than about 600Ω.

Future actions will include actual measurements of simulated configurations with special care of linearity and EMI issues.

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