Tests of the digital demodulation prototype board for the AdV photodiode readout

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Abstract

This note presents the tests made with the prototype of digital demodulation board which confirmed that digital demodulation is a valid option for Advanced Virgo.

Summary

1 Introduction

Digital demodulation has several advantages compared to analogue demodulation. It is a flexible solution with the choice of the demodulation frequency which could be done online. It reduces the amount of analog electronic, especially in the case of multiple demodulations of the same channel. It has a slightly improved SNR compared to analogue demodulation (a factor $\pi/\sqrt{8}=1.11$), thanks to the demodulation with a sine wave instead of a square signal in analogue mixers. It suppresses the phase noise between signals at different frequencies read by the same photodiode, offering the possibility of relaxing the need of the local oscillator distribution.

Digital demodulation is a new technology which becomes available now thanks to the progresses of the ADCs. However, as any new technology, we should check that it behaves as expected. Therefore a test board with the key components for digital demodulation has been built and tested to confirm that this technology is now working. This test board hosts two different types of ADCs to compare their performances and the appropriate FPGA to do the online demodulations.

This note describes the tests made with this prototype of digital demodulation board and presents the conclusion for the use of this technology for Advanced Virgo.

It starts by a description of the prototype boards followed by the first tests made with a simple 10 MHz signal to evaluate the ADCs noise floor and to understand the limitation of the experimental setup. Then it present results with an input signal matching the level of the expected AdV signals. Finally it discusses various techniques to further reduce the phase noise.

It should be stressed that the results of these tests rely on the performances of the test setup, which means not only the performances of the test board, but also the performances of the signal generator used, which limit some of the measurements as we will see. This means that some of the results presented here are upper limits of the noise we could expect with the digital demodulation.

2 Test board description

The test board (see photo below) contains:

- 2 ADCs of different type:
  - ISLA214 which could run up to 500 MHz, but was used only at 400 MHz during the tests, (actually an ISLA214P50)
  - ADS5474 which could run up to 400 MHz.
- One “large” FPGA for on board demodulation (Stratix IV GX)
- IO for usual TOLM output:
  - RJ45 plug for the timing input
  - optical fibers connector for board configuration and data output

Remark: the PCIe connector is not used for the demodulation.

Figure 1 Image of the demodulation test board

3 Software for the test board

The section describes the FPGA demodulation code as well as the two real time PC applications specific to the test board. In additions, usual codes for the timing and data transfer were used by the FPGA and real time PC (RTPC).

3.1 FPGA demodulation

The following figure shows the demodulation scheme used by the test board.

The ADC is triggered by a clock slaved on the timing system. On the same ADC data, multiple demodulation pipelines (shown in light yellow in the figure) could be activated in parallel.

For each pipeline, two signals are produced, one in-phase ("ACp"), one in-quadrature ("ACq"). They are obtained by multiplying the ADC values by a periodic table of sine and cosine values with a frequency being the demodulation frequency (like 6MHz in the figure). The result of the product is integrated over a given number of sample "N" (of the order of 1000), and the result is send at 400 MHz/N (usually 400kHz) to the RTPC for low pass filtering using an 8th order Butterworth filter and further decimation.

The normalisation is such that the demodulated signal gives directly the amplitude of the signal present at the demodulation frequency.

Notice that the periodicity of the sine and cosine tables is independent of the decimation factor N. These tables are used as circular buffer asynchronously from the decimation.

The ADC data are provided as 14 bits number and the table of sine and cosine as 16 bits numbers. The sum of the products is made by the FPGA using 44 bits integers. The result is converted to a 32 bit floating point before sending it to the RTPC.

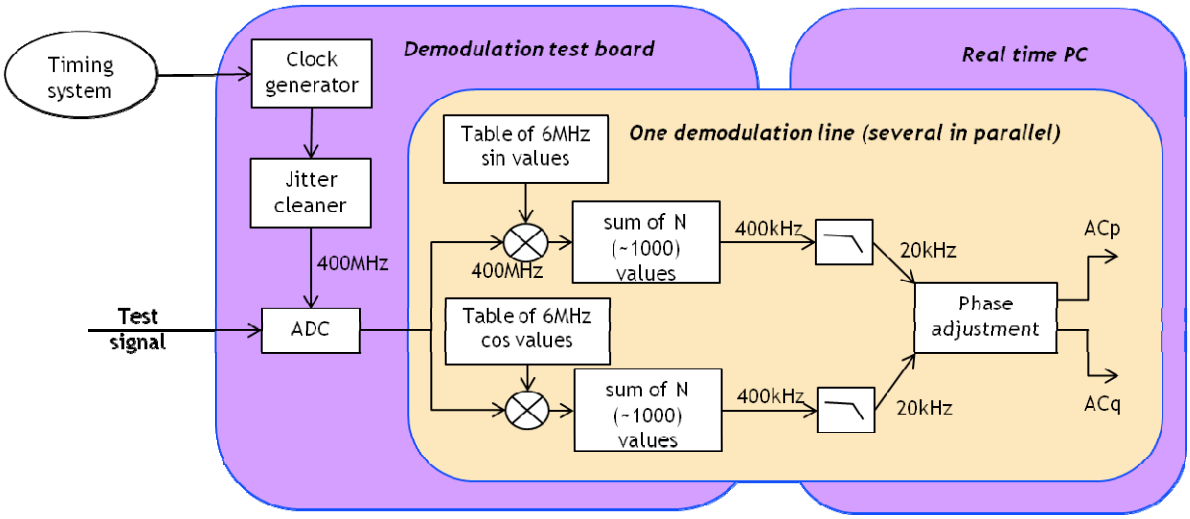

Figure 2 Demodulation scheme implemented in the FPGA and RTPC

In the RTPC, or offline processing, the ACp and ACq could be combined to adjust the demodulation frequency or to do phase corrections.

3.2 TolmAdcProto

This is the application used to look at short segment of full bandwidth data. Since the raw data rate is pretty high (800Mbytes/s for one channel @ 400 MHz), the data could not be send continuously to the RTPC via the optical link. Therefore, in order to be able to see chunk of "raw" ADC data recorded at

full sampling rate, bunches of 32k samples of data are acquired and stored in the memory of the FPGA before being send via the TOLM link to the RTPC were they are archived as frame file. The TolmAdcProto application is taking care of configuring the ADC board, collecting and writing the data. An offline Root macro is then used to display time domain data and to produce spectrums.

3.3 TolmAdcDemod.

This application configures the test board to do the demodulation and to send continuously data packets to a frame builder using the optical link. It performs the following actions:

1. The table of sine and cosine are computed by the RTPC and stored as 16 bits integer using the following code: int data = round (32767 * sin (omega * t + phase)). Since these tables need to be periodic and have a finite size (8k words) not all frequencies are available. Therefore the program searches for the frequency closest to the requested one. The table are then computed and uploaded in the FPGA memory.
2. The PC configure the register of the FPGA to set the clock for the ADC, set the data packet size, and start the processing.
3. The data packets are collected by a TolmFrameBuilder and distributed to a usual Fd pipeline.

Up to 3 frequencies could be used for each ADC channels, with both ADC's used at the same time. This maximum number of 3 demodulation frequencies will be increased in the future.

4 Basic tests

4.1 Noise floor

Figure 3 presents the noise floor for the ISLA214 and ADS5474 ADC, without any conditioning electronic (black curve) and with conditioning electronic (red curve).

The data sheet of the ADS5474 claims 11.2 ENOB on a $2.2V_{pp}$ range which translate to 13.5nV/sqrt(Hz)[1]. For the ISLA214, the ENOB is 11.5.on a $2V_{pp}$ range translating to 10nV/sqrt(Hz). The noise floors measured without conditioning electronic confirm the values given by the data sheets, with the ISLA214 being less noisy than the ADS5474.

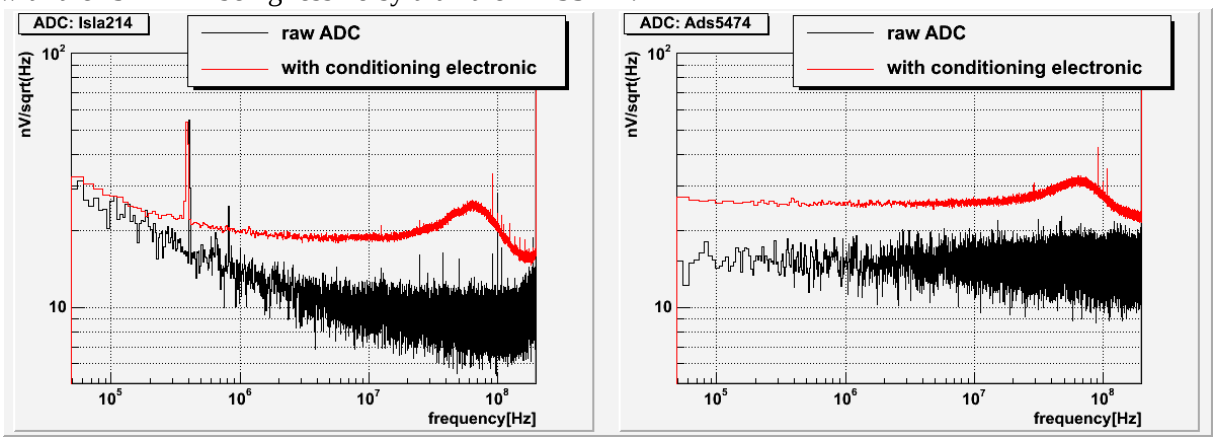

Figure 3 ADC noise floor before (black) and after (red) connecting the analogue conditioning electronic. For both ADCs, the sampling clock was set to 400 MHz

The conditioning electronic includes a stage with a 0.5 gain with a single ended to differential convertor and an anti-aliasing filter cutting at 100 MHz. This conditioning electronic introduce some extra noise, a factor two above the pure ADC noise, due to its non optimal design (especially the 0.5 gain). We expect to remove this noise in the future version of the demodulation board and to reach the raw ADC noise, which means to gain a factor two on the noise floor. Of course, this anticipated gain has not been included in the measurements presented in this note. We could also expect to further reduce the noise floor by a factor sqrt(500/400)=1.12 by running the ISL214 at 500MHz.

Figure 4 presents the noise floor (with the conditioning electronic) measured at different sampling rate. The noise floor varies as the inverse of the square root of the frequency, as expected. For a 400 MHz sampling rate, the noise floor is about 19nV/sqrt(Hz) for the ISLA214 and 25nV/sqrt(Hz) for the ADS5474.

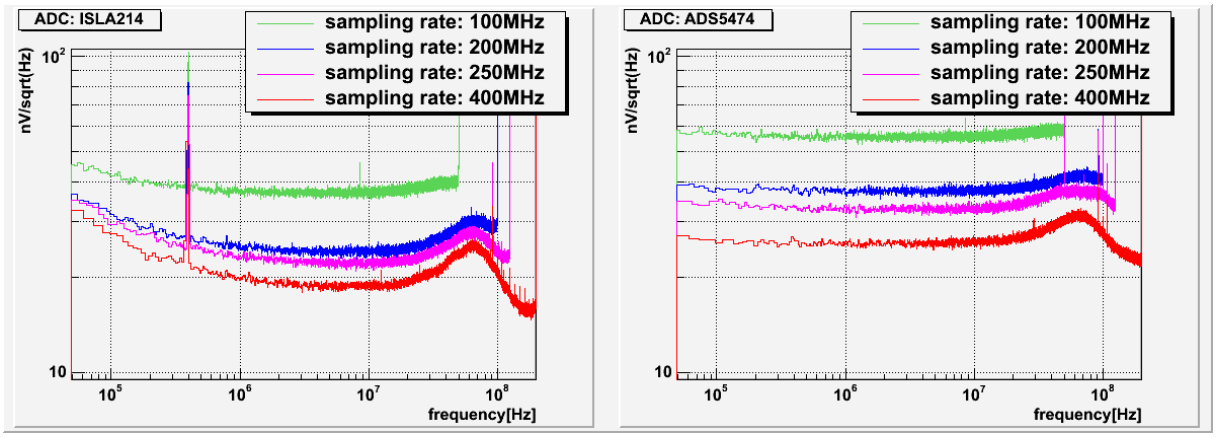

Figure 4 Noise floor for different sampling rates

[1] $2.2V/2^{11.2}/\text{sqrt}(12)/\text{sqrt}(4.e8)=13.5nV$

4.2 Harmonics distortion

To evaluate the distortion generated by the ADCs, a clean line was injected at 6.25 MHz and 56 MHz and the wide band spectrum taken to evaluate the level of the harmonics. The clean line was produced using an IFR2026A signal generator followed by a passive pass-band filter centered on 6.25 MHz (respectively 56 MHz) which removes all harmonics from the input signals. Figure 5 and Figure 6 present the results. In both cases, two data sets are plotted, one with the signal generator set to nominal frequency (black) and a second set (red) with the signal generator set to twice the nominal frequency, but with the same amplitude, keeping the same initial passive filter. The purpose of this second set is to show that the pass-band filter is indeed filtering the signal much more than the observed harmonic distortions. In both cases, the ADC was running at 400 MHz.

The observed level of harmonic is compatible with the level from the data sheet for the 6.25MHz line (between 80 to 100dB), but worse for the 56MHz case (around 60dB). Nevertheless, this is not a problem for our application since the most sensitive frequencies are not harmonics of the loud 2f signals. The leakage from the 6MHz to 56MHz is attenuate by about 90dB, a factor large enough to avoid any pollution of the useful signal bandwidth.

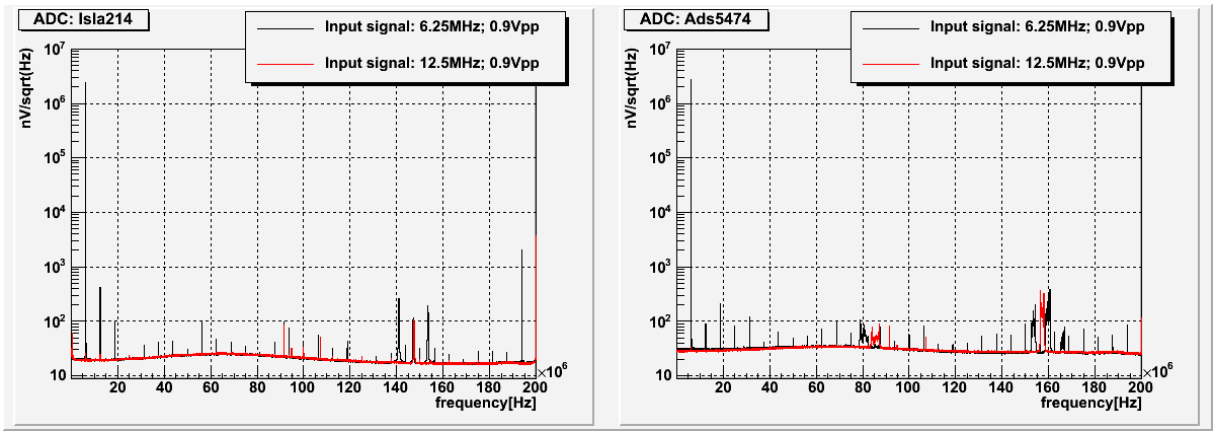

Figure 5 Non linearity test with a 6.25MHz line. See text for details

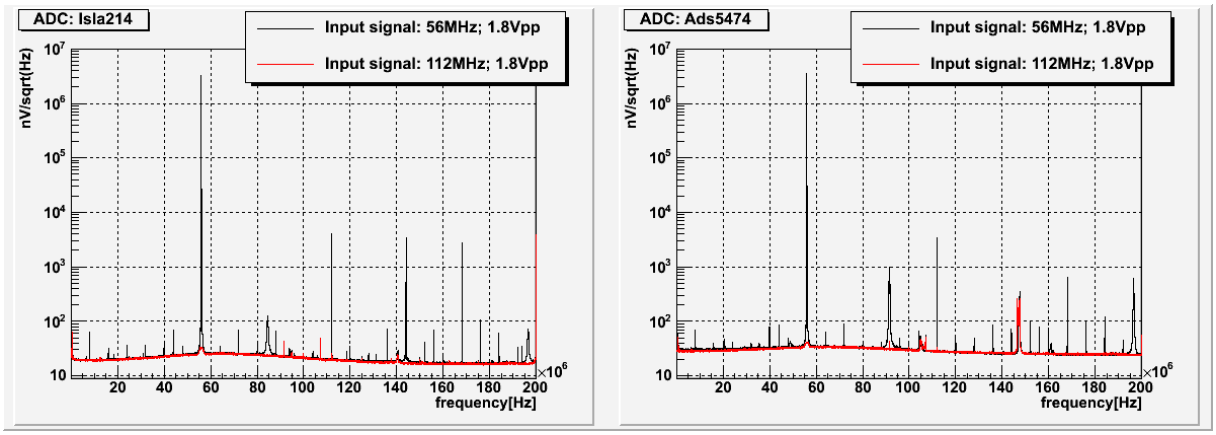

Figure 6 Non linearity test with a 56 MHz line. See text for details

4.3 Temperature

The demodulation board will be implemented as mezzanines in the DAQ box were no fans are foreseen to reduce the acoustic noise. Therefore the thermal load is an issue and heat load should be minimized.

The following images show a thermal view of the prototype board sitting flat on a table without fan. Without surprise, the ADC ADS5474 which dissipates 2.5W according its data sheet is the warmest component with a temperature of 97°C above its maximum operating temperature (85°C).

The operating temperature of the ISLA214 is around 65°C, a much reduced value thanks to its smaller power need: 835mW according its data sheet.

Figure 7 Left: regular image of the test board. Centre: thermal image with the ADS5474 turned on. Right ISLA214 turned on. The white and blue circles indicate the positions of the ADS5474and ISLA214.

Of course, a radiator will be placed on top of the ADCs, but this test confirms without surprise that the ISLA214 is the preferred choice for the thermal load point of view.

5 Test with 10 MHz signals.

To investigate the ADC noise around a strong line, a 10 MHz signal was generated, and then demodulated with the on board FPGA, followed by a low pass 8th order Butterworth filter cutting at 8kHz before down sampling the signal at 20kHz.

5.1 Measurements with different signal generators

Since the measured noise could come either from the signal generator or from the ADC board, three different signal generators were used:

- An IFR 2026A general purpose signal generator.
- An independent standalone atomic clock.
- A 10 MHz clock generated by the test board itself, derived from its own internal clock. This clock should have a lower phase noise compared to the 400 MHz ADC clock since it is derived from the same internal clock.

All clocks were delivering a signal around 1Vpp within less than a factor 2.

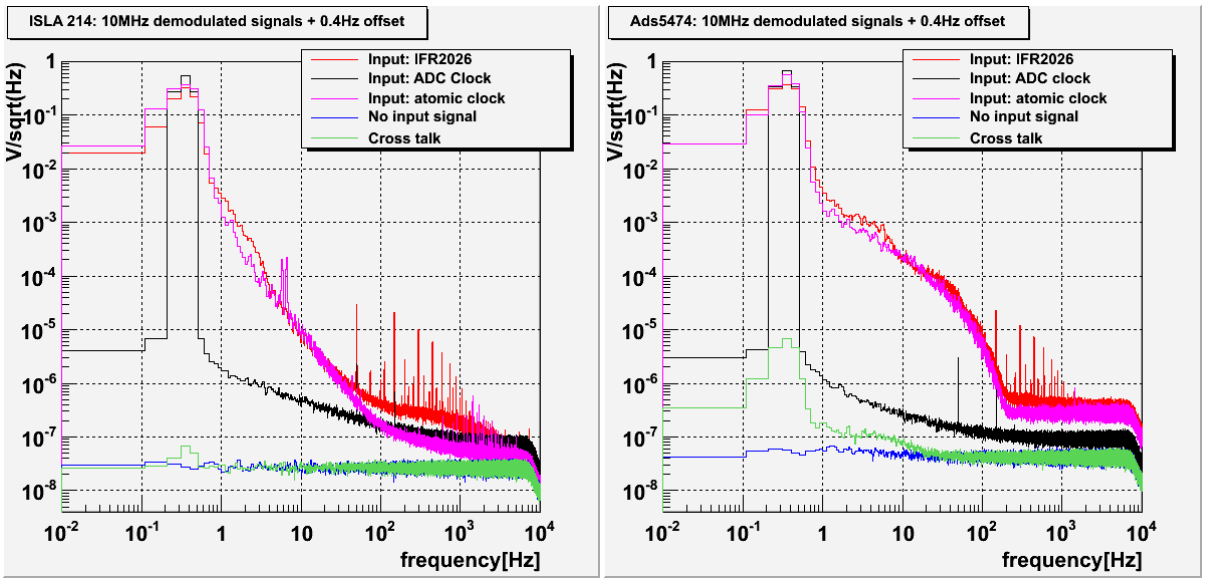

Figure 8 Demodulated signals for various signal generators. All inputs signals are at 10 MHz. The cross talk is measured without signal on the ADC, but with the loud 10 MHz signal on the second ADC of the test board.

Figure 8 presents the results of this test. A 0.4 Hz frequency offset was added offline by combining the in-phase and quadrature signal to see the amplitude of the injected line. Several comments can be made:

- The ADS5474 has some extra noise in the 1-100 Hz frequency band and also above 200 Hz.
- The noises observed with the IFR2026 and the atomic clock are very similar below 30 Hz suggesting that the noise is coming from the test board in this frequency band. The clean signal with the test board clock indicates that this noise is due to phase noise between the test signal and the test board clock. This is further investigated in section 5.3.
- Above 30 Hz, the ISLA214 has a lower noise floor with the atomic clock signal, indicating that we are dominated by the IFR2026 noise, including some 50 Hz and harmonic lines which are not visible in the spectrum of the atomic clock.

All this measurement underlined that the measured noise could sometime come from the signal generator used to test the board and not from the board itself. Some of the presented measurements are therefore just upper noise limits.

5.2 Comparing the ISLA214 and ADS5474 noises

To better understand the differences between the ISLA214 and ADS5474, the "same" 10 MHz signal (using two output of the IFR 2026Asignal generator) has been sent to both ADCs, the demodulated signal recorded (without any frequency offset), the amplitude and phase noises extracted and their coherence computed (see Figure 9).

As already commented, the ADS5474 has some extra noise, especially for the amplitude. The phase noise is however more coherent between the two ADCs than the amplitude noise, which is another indication that there is some phase noise at the level of the onboard clock and/or signal generator.

The fact that the ADS5474 has some extra noise combined with its extra thermal load **made the ADS5474 a second choice and therefore the further investigations have been focused on the ISLA214**.

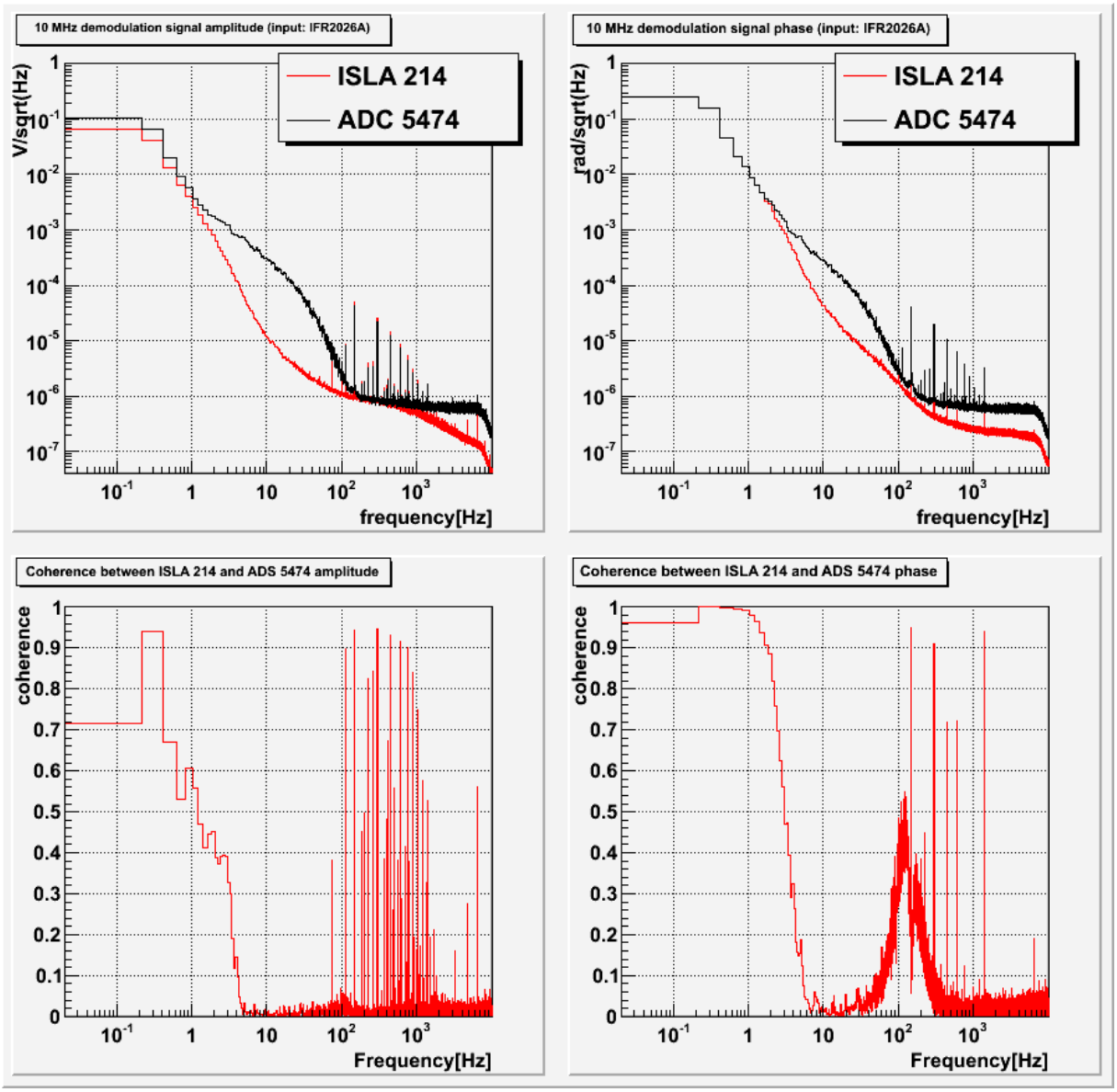

Figure 9 Amplitude noise (left plots) and phase noise (right plots) for the ISLA214 and ADS5474. Bottom plot: coherences between both ADCs.

5.3 10 MHz measurements and phase noise.

To investigate the origin of the noise below 30 Hz, measurements were made with different clock synchronization conditions. Figure 10 shows the various setup used. For these tests, the signal generator amplitude was tuned to match the amplitude of the onboard clock. Figure 11 presents the results which show that if we bypass the IRIG-B distribution to the test board clock (blue and green curves), the noise floor is significantly reduced confirming the hypothesis of some phase noise at the level of the test board. The following section will discuss the origin of this phase noise.
These plots, especially the green one also shows that the phase noise signal generator is of the order of 10^{-4}V, or roughly 90dBc, below a few Hz.

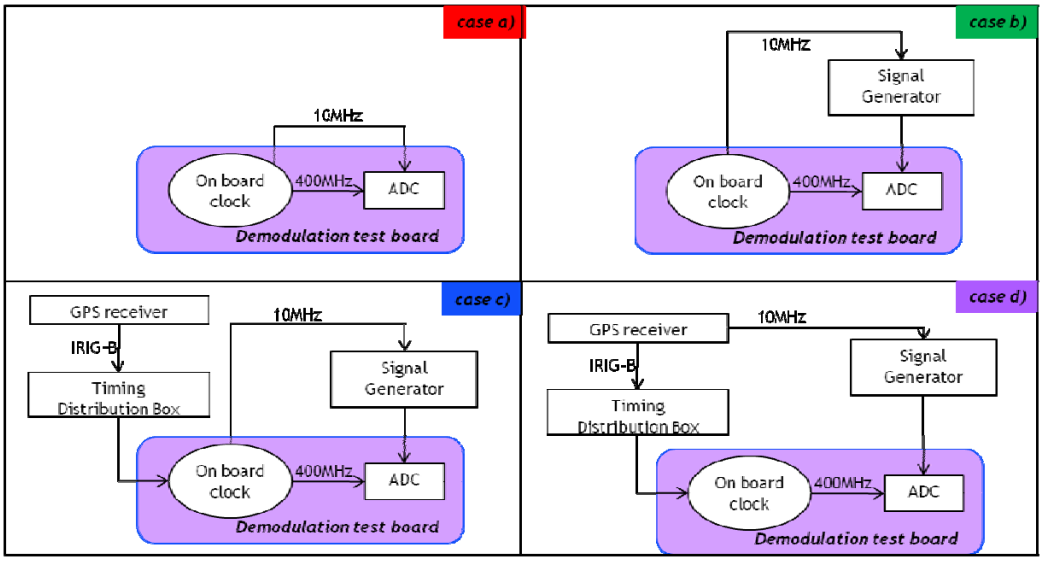

Figure 10 various setups used to measure the phase noise around a strong 10 MHz line. The colours of the label match the colour of the line in the following figure

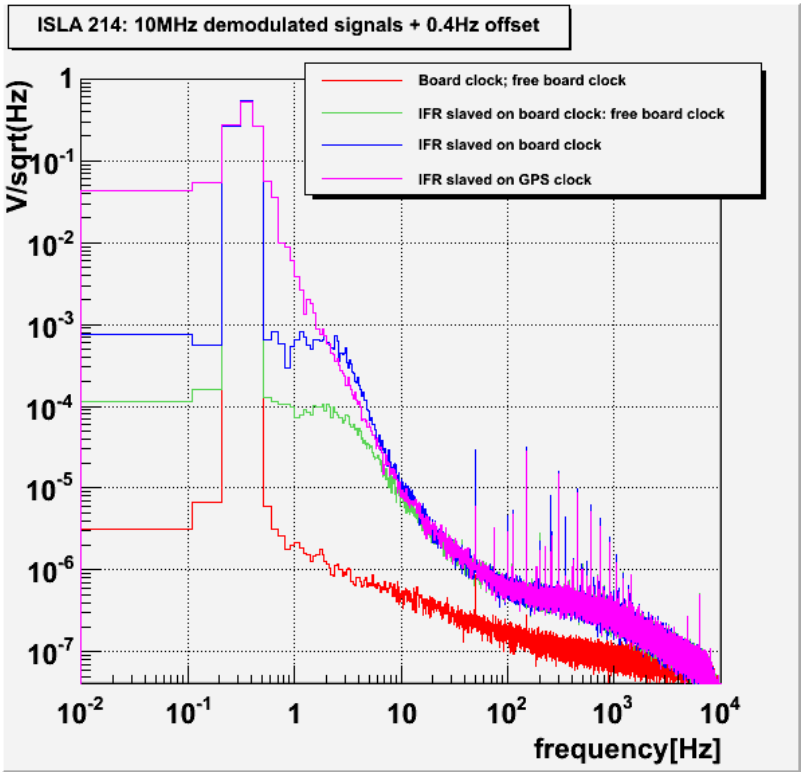

Figure 11 Results of the tests made to investigate the phase noise.

To emphasize that part of the noise spectrum is driven by phase noise of the test board, measurements were made at different frequencies with the usual configuration (case “d” of Figure 10). The results are presented in Figure 12. We can see that below 10-30 Hz, the noise is just proportional to the frequency, indicating a linear coupling as it should be for frequency noise. Above this frequency, the shape of the noise curve changes, indicating some different noise (phase or amplitude) from the signal generator.

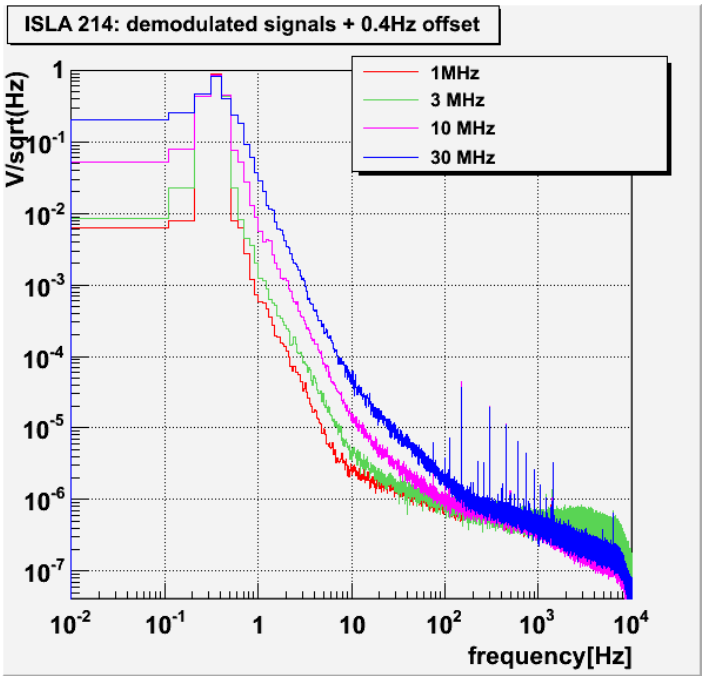

Figure 12 Spectrums of the demodulated signal for different modulation frequencies

5.4 Phase noise of the test board clock

The onboard clock of the test board is usually slaved on the GPS clock using the IRIG-B signal. The IRIG-B provides a 1PPS signal (which is used for the Virgo+ ADCs and TOLM) but also a 100 Hz signal which is used for this test board. The errors signal is extracted by sending the IRIG-B signal to one FPGA input, which means that the timing offset is measured with just the resolution of the FPGA tic clock: 10ns. A simple PID[2] is then used to slave the TCXO of the test board using a DAC.

Figure 13 presents few seconds of typical data. The blue trace shows the measured time offset and the black curve the DAC values. The red trace is the phase extracted from an 8MHz signal (the test configuration is still the case “d” of Figure 10) which allows a continuous accurate monitoring of the TCXO phase compared to the GPS phase. From this plot one can easily see that the limited resolution of the TCXO phase offset measurement by the FPGA allows a “large” phase noise of the order of a few ns at low frequency. The TCXO is actually most of the time uncontrolled.

This was not a problem for the Virgo+ ADCs, given the frequency of the signal considered, but this will be improved on the demodulation board by digitizing the IRIG-B signal with an ADC, instead of using a simple threshold like it is done now by the FPGA.

To show the level of accuracy of the phase noise, Figure 14 show the spectrum of the error signal (“integral”) with the loop open (purple curve) or close (black curve).

[2] the values used for the tests are 0x12 x10 0x0

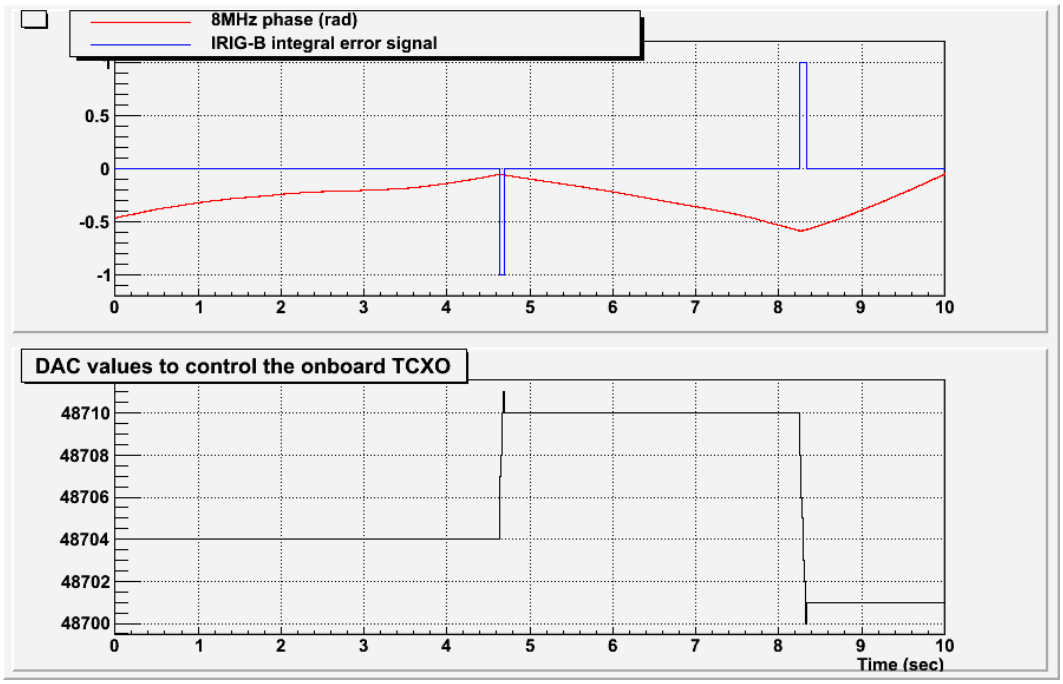

Figure 13 Typical example of the phase noise of the onboard TCXO and DAC values used to slave it

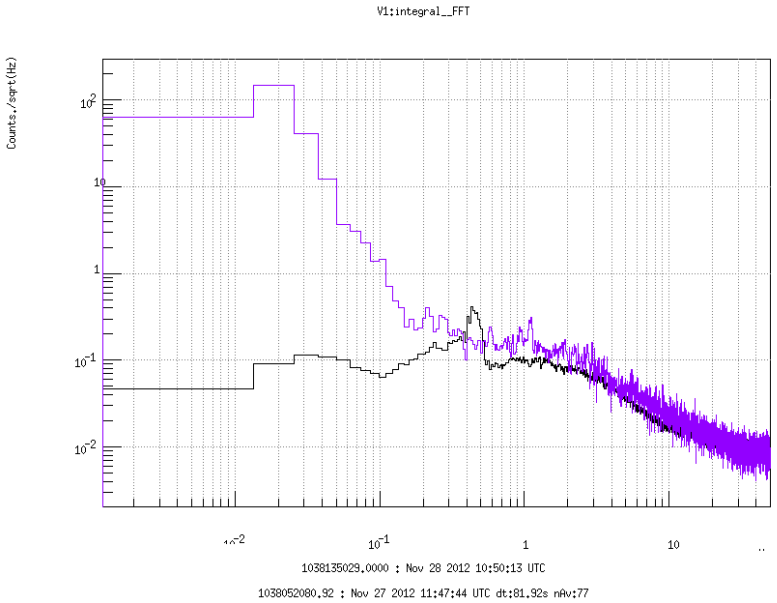

Figure 14 Phase noise of the onboard TCXO when the feedback is off (purple curve) or on (black curve). The vertical unit is 10ns

6 Test with expected photodiode signals

To best use the flexibility of digital demodulation, the ADCs should have a broadband input. But the photodiodes RF signals have some spectral components with fairly high amplitudes due to the signals at twice the modulation frequencies (the "2f signals"). This will put severe constrains on the ADC which digitize the full bandwidth and therefore could limit the observable noise. The purpose of this section is to evaluate the use of digital demodulation with such large signals.

6.1 Expected signals

The following table summarized the expected signal for the most challenging beam, i.e. for the beam with the largest amplitude. Thanks to the DC readout of AdV, the dark fringe signal which is even more challenging when using AC readout is not part of this list. The powers are extracted from the VIR-0472A-12 document. See comments below for more explanations.

Type of signals	**Demodulated signal amplitude on one photodiode**	**Voltage at ADC input**
Shot noise for 50mW DC	0.137nW /sqrt(Hz) [(a)]	54 nV/sqrt(Hz) [(b)]
Amplitude of the loudest signal used in science mode (f_3 for B2)	11 μW_{pp} [(c)]	4.6mV_{pp}
Amplitude of the loudest signal when doing large injections (f_3 for B2)	110 μW_{pp} [(c)]	46mV_{pp}
Amplitude $2f_1$ taking into account a factor 2 attenuation from the preamplifier notch.[(d)]	1.1 mW_{pp}	456 mV_{pp}
Amplitude $2f_2$ taking into account a factor 2 attenuation from the photodiode response	0.8 mW_{pp}	332 mV_{pp}
Amplitude $2f_3$ taking into account a factor 2 attenuation from the preamplifier notch.	1.1 mW_{pp}	456 mV_{pp}
Sum of all signals in science mode for the most challenging beam: B2.	3.1 mW_{pp}	1.3 V_{pp} [(e)]

Comments:

a) This is the noise level after demodulation of a 50mW beam: $ShotNoise = \sqrt{2}\sqrt{Ph\nu}$ with P=0.05W. It assumes a 100% quantum efficiency and takes into account a $\sqrt{2}$ demodulation factor. The demodulation normalization has been chosen to output directly the amplitude of the input signal.

a) The raw ADC noise = 19nV/sqrt(Hz), or 27nV (19*sqrt(2)) after demodulation Since we want to have the shot noise a factor 2 above the signal, the gain should be such that the shot noise amplitude is 2*sqrt(2)*19=54nVpp. **Therefore the trans-impedance gain is 54nV/0.13nW = 415V/W** for this column.

b) See B2 f_3_P values in table 7 of VIR-0472A-12.

c) We intend to have a lose notch around 14MHz to attenuate the 12 and 16MHz lines by about a factor 2, in order to reduce the overall signal dynamic.

d) The total voltage is below the 2Vpp range of the ADC. Actually a factor two of margin should be gained: as explained in section 4.1, the noise floor of the test board is not dominated by the ADC noise (a factor 2 lower) but by the extra noise coming from the prototype conditioning electronic which will be reduced in future version.

6.2 Test conditions

A test signal was generated with the IFR 2026A. The generator was synchronized on the timing system using the 10 MHz output from the GPS receiver. The signal generator was generating simultaneously three signals and doing internally their sum. The test signal was the sum of the following amplitude:

4.6 and 46 mVpp at 8361036 MHz (f_3)
456 mVpp at 12.541554MHz ($2f_1$)
456 mVpp at 16.722072MHz ($2f_2$))

Two different conditions for the f_3 amplitude were used: one for the science mode condition and one with the extra loud lines, a factor 10 higher.

Figure 15 shows this signal as seen by the ADC. Although only three lines are requested, some extra lines are present, especially the harmonic of the 12 and 16 Mhz. This is probably due to the signal generator producing a complex signal with three lines, since it is larger than the result of the ADC distortion test reported in section 4.2.

The noise floor is also slightly higher compared to the noise floor reported at the beginning of this note. This is due to the signal generator which produces a wide band noise. This is expected given the large dynamic of the signals requested. The effect of the wide band noise produced by the signal generator is visible on Figure 16 which shows the observed noise produced by the signal generator using or not a passive analog pass-band filter (red curves). The black curve, with the excess noise, corresponds to the case without the filter, but with just an RF attenuator to match the signal amplitude of the pass-band filter case.

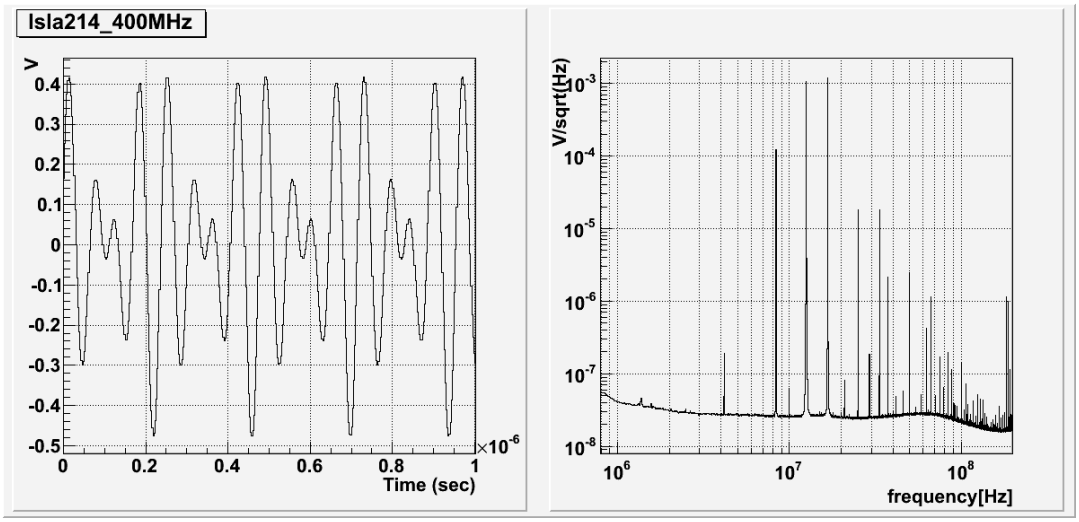

Figure 15 Test signal: left in the time domain, right spectrum.

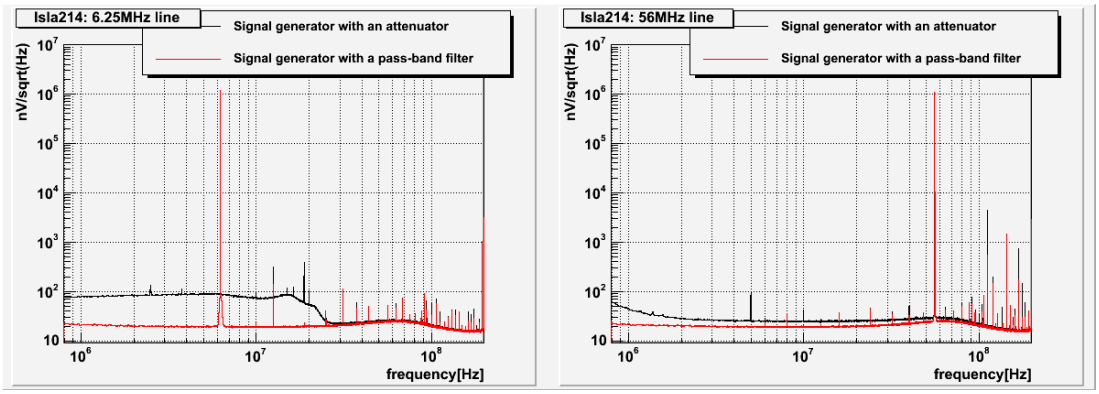

Figure 16 Wide band noise from the signal generator (black) compare to a filter signal (red)

6.3 Demodulation frequencies

The following table gives the list of the parameters for the demodulation. The approximated frequencies are given by the formula:

$$f_{approx} = 400 \text{ MHz} \times N_{period} / N_{samples}$$

Target frequency (Hz)	Approximated frequency (Hz)	Frequency Offset (Hz)	Number of sample for the sine and cosine tables	Number of periods in the tables
6270777	6270783.847	6.847	2105	33
8361036	8361045.130	9.130	6315	132
12541554	12541567.695	13.695	2105	66
16722072	16722065.967	6.032	7822	327
56436993	56437002.470	9.470	3643	514

The decimation factor was 1000 and the ADC sampling rate 400 MHz.

6.4 Data with using only one ADC channel

Figure 17 presents the raw demodulated signals in the time domain for the three injected frequencies. A large oscillation due to frequency offset between modulation and demodulation frequencies (see above table) is well visible. The amplitude of the demodulated signal is compatible with the injected lines, showing that the demodulation procedure implemented in the FPGA is working properly.

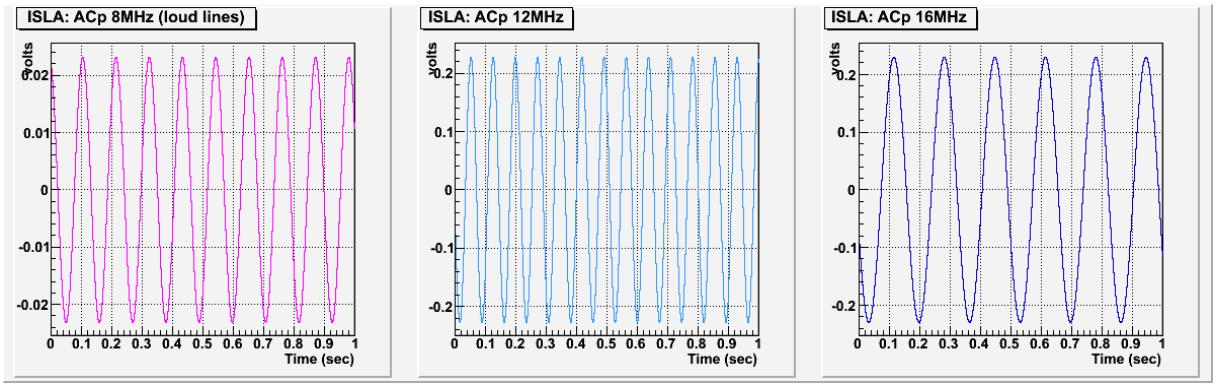

Figure 17 Demodulated signal in the time domain

Figure 18 presents the spectrum of the same signals as well as the spectrum of the signals at frequencies where no line was injected. The frequency offset correspond to the above table.

The first correction is to remove this static frequency offset Δf by combining the ACp and ACq signal as function of time:

$$AC'p(t) = \sin(\omega t)ACp(t) - \cos(\omega t)ACq(t)$$
$$AC'q(t) = \cos(\omega t)ACp(t) + \sin(\omega t)ACq(t)$$
$$With\ \omega = 2\pi\Delta f$$

Figure 19 present the results of this operation for the same data. A 0.4 Hz has been kept to highlight the input signal amplitude and have the full dynamic. Thanks to this slight frequency offset, the ACp or ACq spectrum are the same and we are reporting only one of them.

A few remarks:

- This data shows that the signal which must be shot noise limited, the 8MHz signal with the science mode amplitude, is indeed below the shot noise level above 15Hz, which is a frequency smaller than the critical frequency where the control signal may pollute the sensitivity (above 30 Hz, see figure 8.3of the TDR). This proof that digital demodulation is working, and even with loud signals at the 2f frequencies, we can keep the key science mode signals below shot noise as expected.

- The noise floor is slightly higher than the electronic noise. This is due to the signal generator which produces a wide band noise, has already highlighted in section 6.2. This is an artifact of the test setup, not of the demodulation board itself.
- The loud 8MHz signal and the 2f signals are showing some extra noise, due to generator noise and the phase noise of the test board. This will be discussed later on.
- The other high frequency channels (6 and 56 MHz were no signal was injected) are basically free of noise.

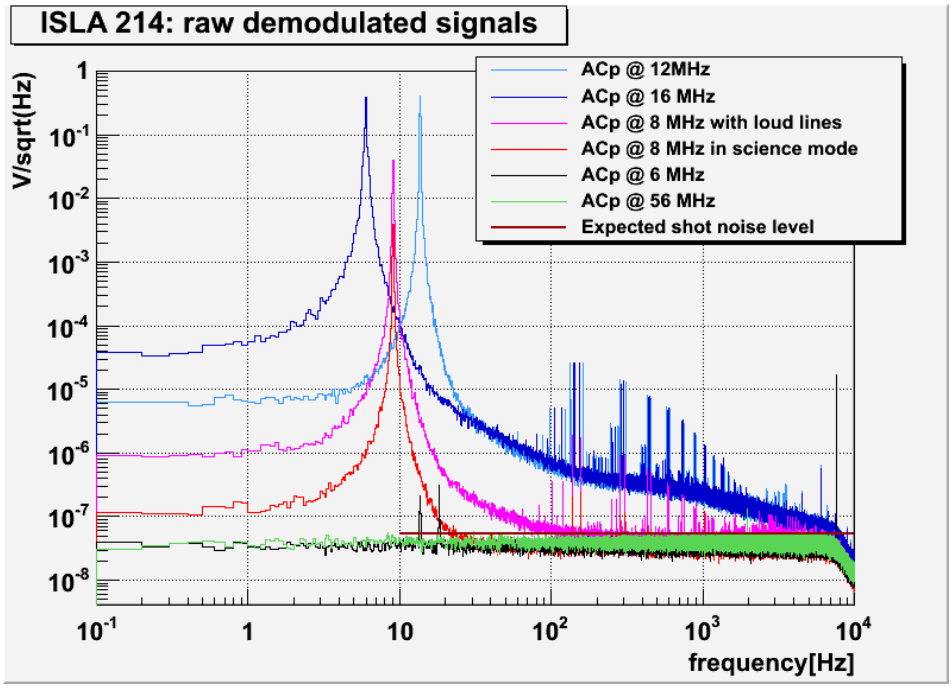

Figure 18 Raw demodulated signals

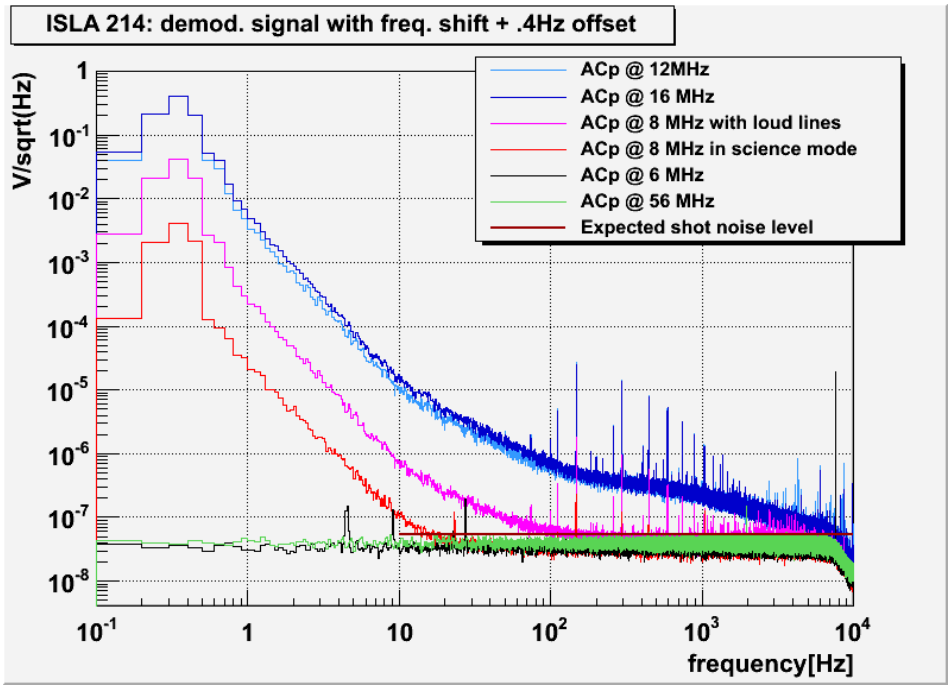

Figure 19 Demodulated signal after correcting for the static frequency offset. A 0.4Hz offset has been kept.

6.5 Reducing phase noise using the second ADC

In order to see the impact of the phase noise, the 10 MHz signal from the GPS receiver was digitized by the second ADC on the test board the ADS5474. Figure 20 present the layout of the cabling for this measurement. The ADS5474 data are then demodulated at 10 MHz in order to extract a phase noise which is then used to correct the phase of the ISLA214 signals.

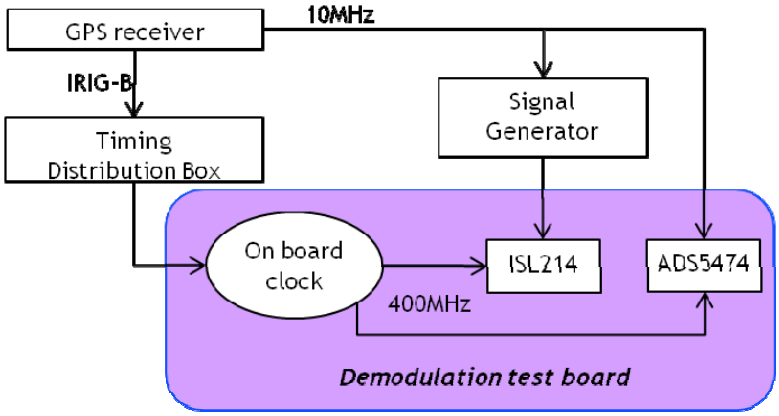

Figure 20 Clock layout for the tests with the second ADC

Figure 21 presents the spectrum once this correction is applied, in addition to the static frequency offset. A strong reduction of the noise below a few Hz is observed as we can expect since the onboard clock noise in this band is due to the poor IRIG-B time offset resolution (10ns). The level of noise at low frequency is compatible with the expected noise of the signal generator, has estimated in section 5.3, see Figure 11. This indicates that this measurement is limited by the signal generator itself and not by this noise cancelation technique.

Above a few Hz, the noise is increased compared to the solution without phase correction. This is not surprising since the ADS5474 is noisier compared to the ISLA214 (see Figure 9). This effect should not be present in a proper implementation with a better second ADC, which could run only at a few 100kHz.

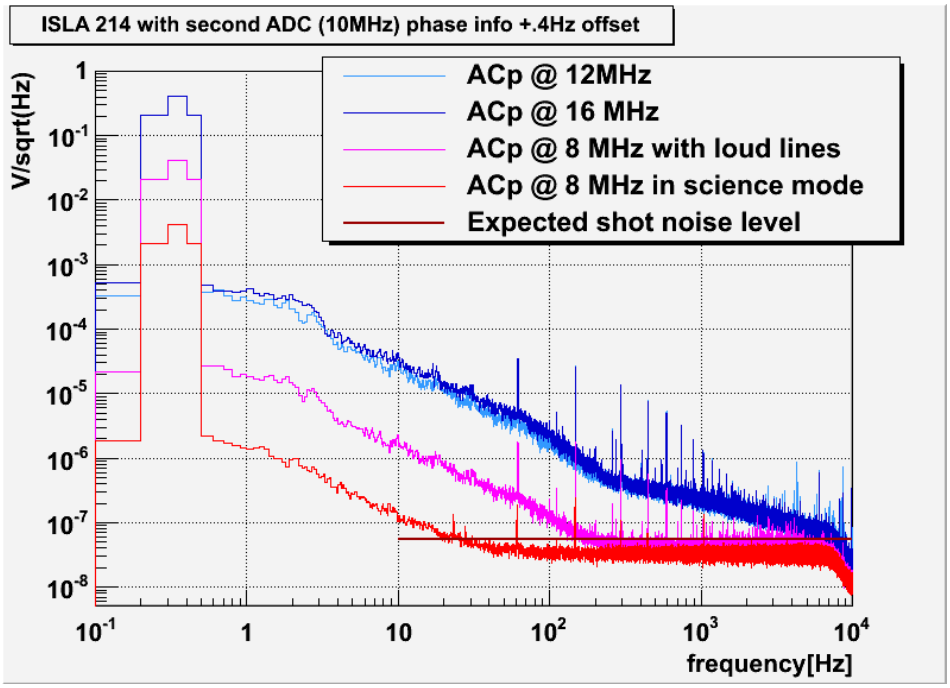

Figure 21 Spectrum with signals corrected for the static frequency offset plus the phase noise using a measurement from the second ADC

6.6 Reducing the phase noise with the 2f signals

One of the main benefits of the digital demodulation is that all signals are acquired by the very same electronic. This means that any phase noise of the ADC board will be seen by all demodulated signals. Figure 22 is showing this effect. It presents the phase noise of the 8 MHz signal, the phase noise of the 16 MHz signal, divided by 2 to be compared to the 8 MHz signal, and their differences. As we can see, both signal measured the same noise; the 8 MHz begin noisier because its amplitude is weaker.

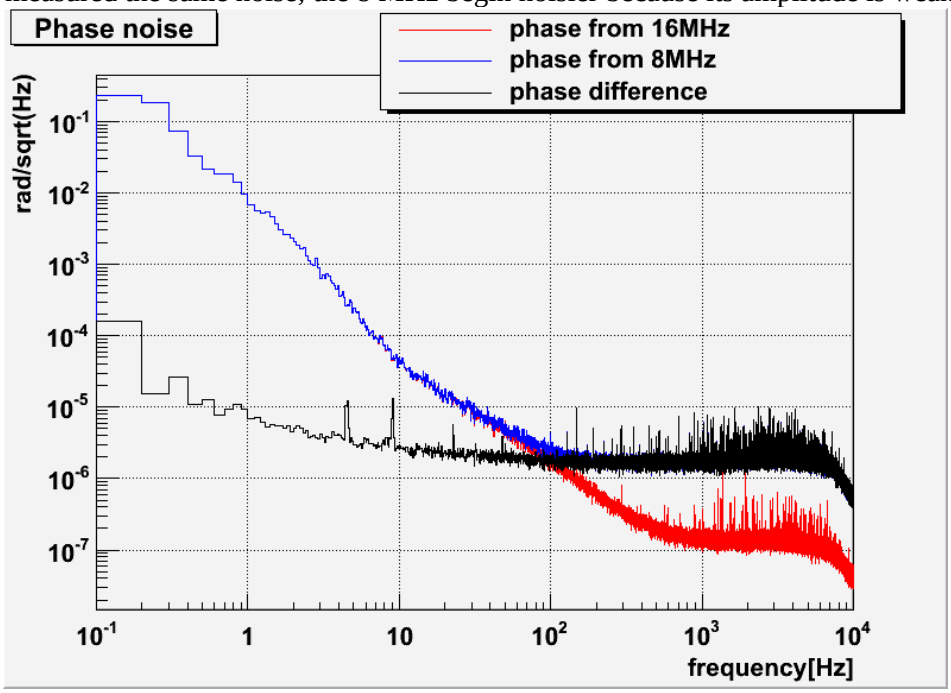

Figure 22 Phase noise of the 8 and 16MHz signal

Therefore we can use one of the demodulated signals, typically a 2f signal as a clock reference to remove phase noise. Figure 23 presents the result of this operation. The remaining noise is expected to come from the amplitude noise of the signal generator as it has been described in section 5.1 when comparing the signal from the IFR2026A signal generator and the atomic clock signal.

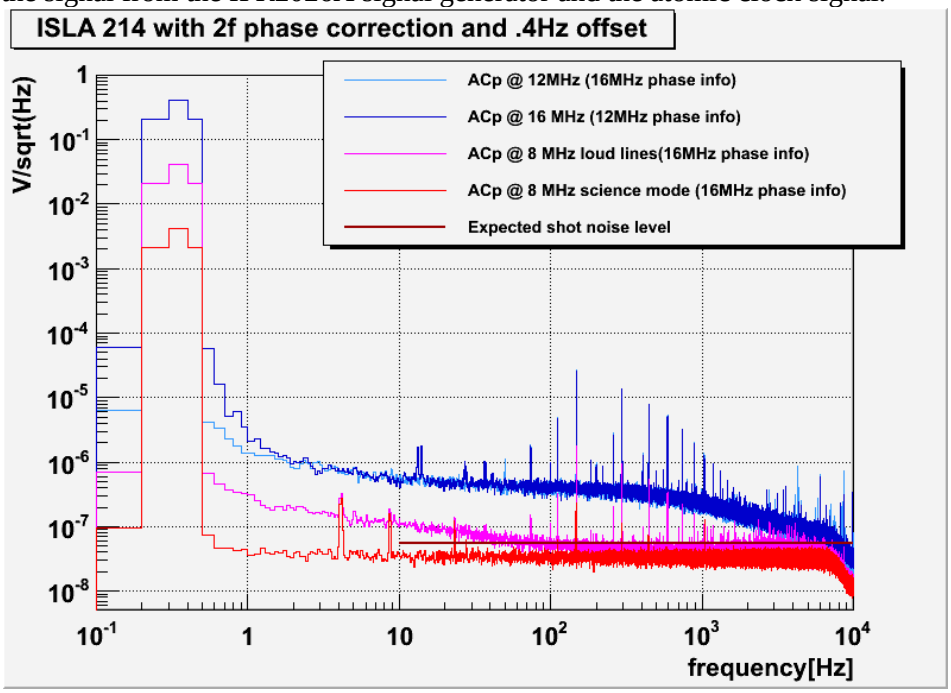

Figure 23 Spectrums with static frequency offset corrections plus phase correction using the 2f signals

Using the 2f signal to reduce phase noise might look unsafe at first thought. However, the 2f signals, which measure the side band power, are needed during the lock acquisition phase. Once the interferometer is locked, these signals are pretty stable; otherwise, they would pollute the demodulated signals which are the product of the sideband and carrier. This stability is shown on Figure 24 which presents the phase noise of the B5_2f signal (red plot). Above 10 Hz, this signal is well below 10^{-6}, and would indeed provide the phase noise improvement level better than the one presented in Figure 22.

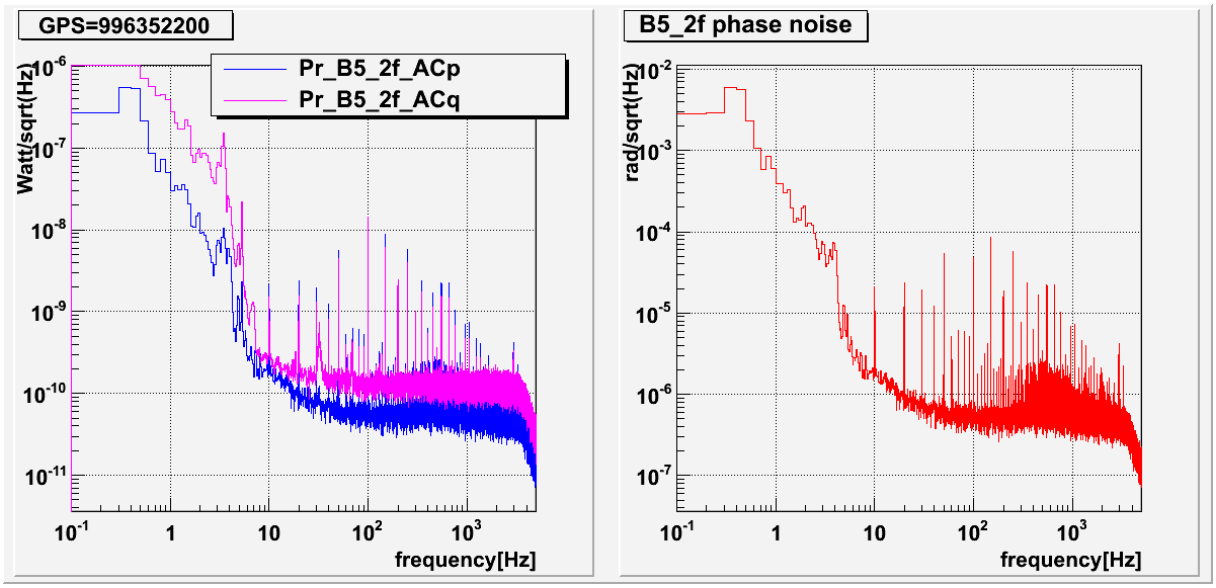

Figure 24 Left: spectrum of the Pr_B5_2f signals. Right: phase noise of the 2f signal extracted from these two signals. Data are from VSR4

Such a schem has already been tested in LIGO, where the ususal RF oscillator distribution system was replaced by a local generation using the 2f signal[3]. Both ways of controling the interferometer gave simillar results confirming that this technique could be used on real interferometer.

Notice that since all modulation frequencies are coming from the same generator, we will have several measurements of the phase noise with the $2f_1$, $2f_2$, and $2f_3$ signals, and it will be possible to select the less noisy one.

[3] Nicolas Smith and Daniel Sigg LIGO-T050138-00-D
https://dcc.ligo.org/cgi-bin/private/DocDB/ShowDocument?docid=27506

7 Summary of the test for the 8MHz signal and conclusions

Figure 25 presents the summary of the measurement made for the expected 8 MHz signals. The left plot is showing the science mode case where the signal is below the shot noise level above about 10 Hz, even just with the existing timing system. This confirms that digital demodulation should work for AdV.

Some excess of noise is observed in the right plot of Figure 25 which corresponds to the case of loud injections. As explained in this note, part of this noise is coming from the noise of the onboard clock which will be improved, thanks to the digitization of the IRIG-B signal. The purple curve is showing an upper limit of this technique, which is limited at low frequency by the signal generator used for this test, and at higher frequency by the extra noise of the ADS5474.

The phase noise subtraction with the 2f signals (red curves) let us suppress most of the phase noise. The measurements are then dominated by the amplitude noise of the signal generator. Anyway, in this condition the results are closed to the shot noise level and let us expect that even for these loud signals, we could be shot noise limited.

Finally, although the 2f phase noise cancelation technique is appealing, this technique is not required to provide shot noise limited science mode control signals. This is a bonus for the cases of loud signals and will help us investigating the effect of the sideband amplitude and phase noise when doing the commissioning of AdV.

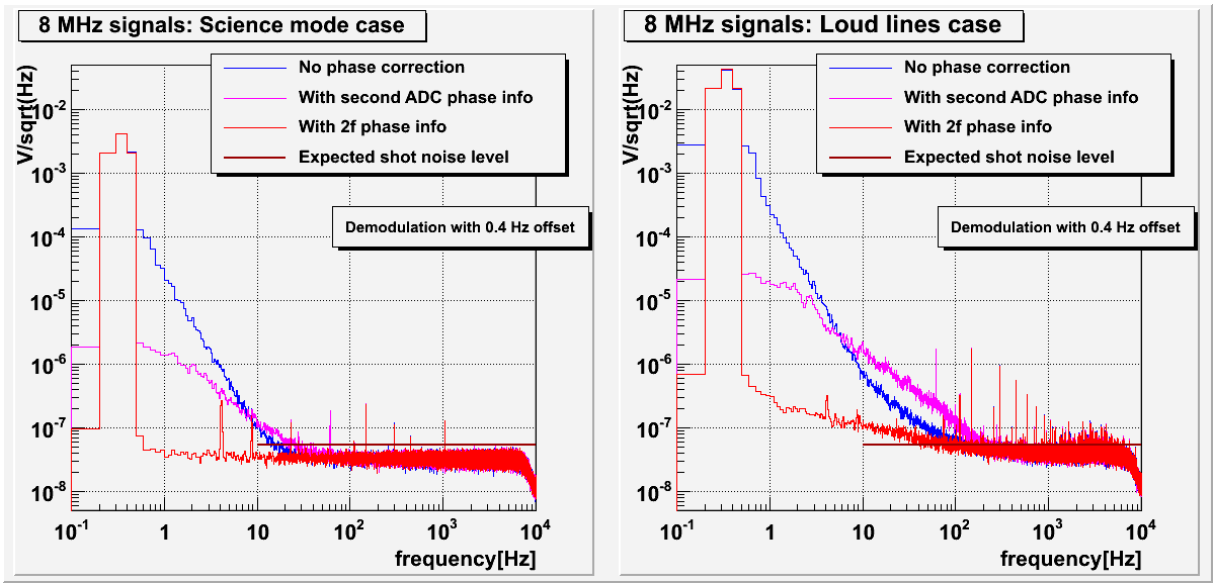

Figure 25 Noise of the demodulation of the expected signal for the control signal in science mode (left) and when doing some loud line injections (right)