Super Attenuator Control System

Activities Report

Alberto Gennai (INFN Pisa)

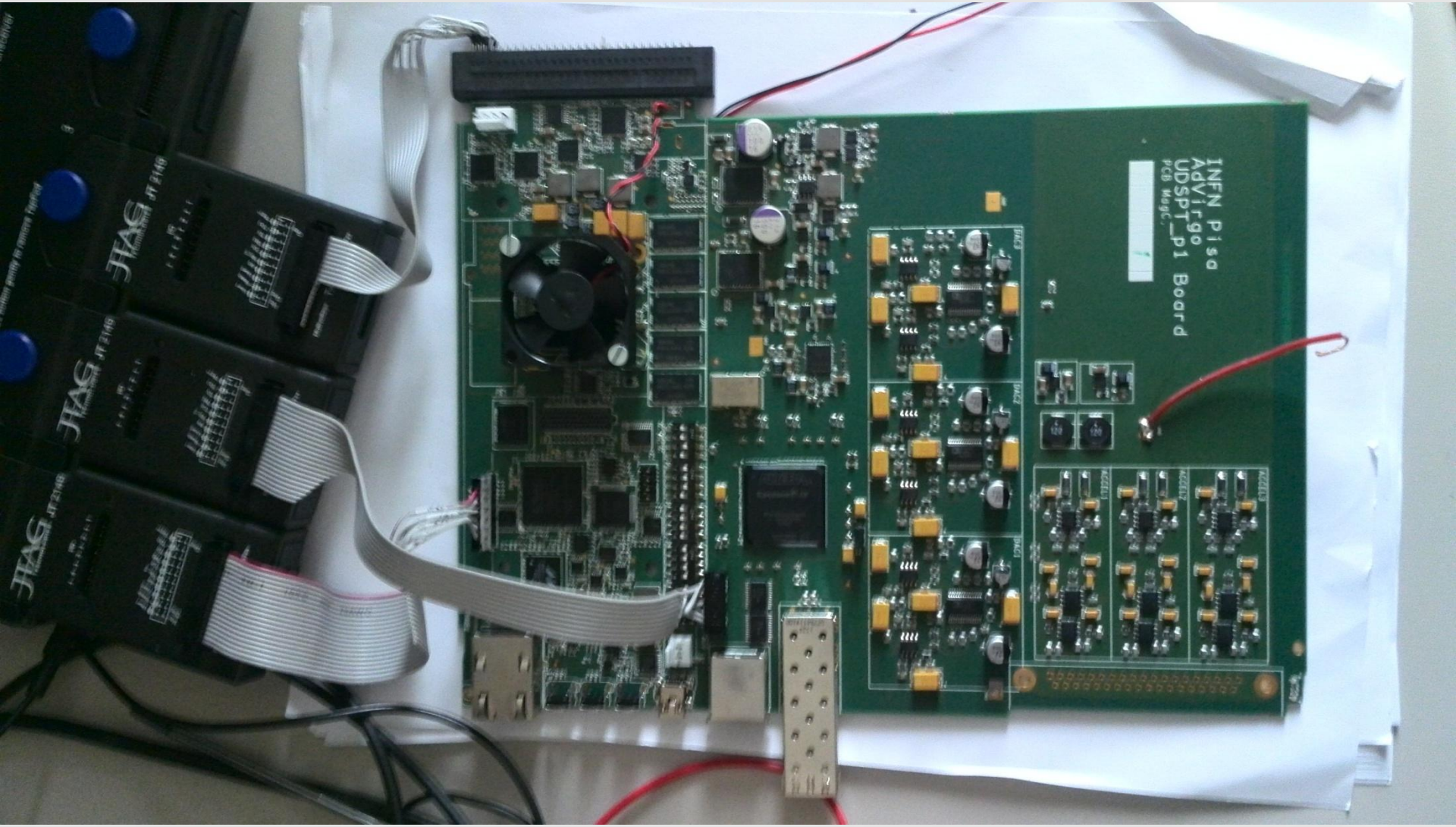
Team

- D. Passuello (INFN Pisa)
- A. Gennai (INFN Pisa)
- C. Magazzu (INFN Pisa) – HW des. & dev.
- V. Boschi (University of Pisa) - Controls
- M. Bitossi (EGO) – HW & FW des. & dev.
- C. Carissimi (EGO) – HW des. & dev.

- EGO support for HW/SW
- L. Rei support (INFN Genova) – SW

Status Report 1/2 (Hardware)

- Boards
  - A second version of electronic hardware was delivered at the beginning of August and test started at the end of the month (4 boards available: 1 under test today probably 2 under test next week).
  - Boundary scan test is in progress and will be the main activity related to boards together with on-board PCIe link in the next few weeks.
  - TOLM interface test will follow
- Other Activities
  - We made few preliminary tests on a different DAC that allows using an external Vref that could be less noisy at low frequency. Test will go on in the next few months
  - We build a small board for testing two alternative solutions for ‘cable-B’ (from distribution frame to boards).
  - We build a small test board for a new high-power section of coil drivers


INFN Pisa
AdVirgo
UDSPT_P1 Board
PCB Magic

Status Report 2/2

- Software
  - Work is proceeding well on DSP compiler and server side. “Damping” porting on new platform is complete. New features are under development and test.
  - We are still in a preliminary phase for what concerns supervisor
- Orders
  - Crates purchase request in preparation.