

# The New High Performance Suspension Control System For Advanced Virgo

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for the VIRGO Collaboration



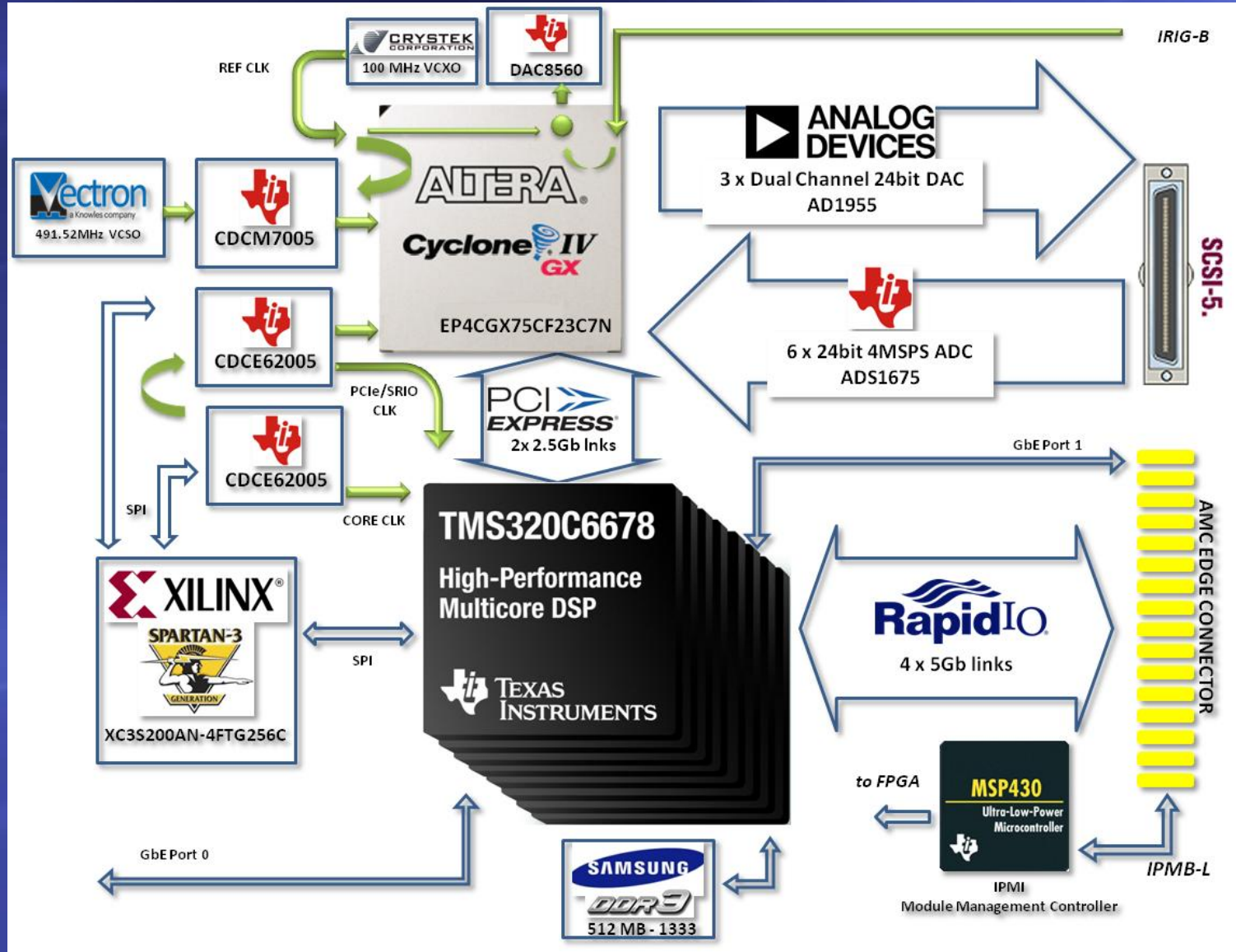
# Motivations & Main Goals

- The old VIRGO Suspensions control system has been in operation since last century (1998)
- In the past we replaced processing units (DSP-based) but we keep on using old front-end analog electronics and data converters (still in use today for some installation task, 17 years after production).
- Few design drivers:
  - Move out of VME standard (limiting board-to-board communication bandwidth)
  - Eliminate physical gap between analog front-end and data converters (in average more than 40 meters STP cabling, multiplied by about 100 signals for each of the 10 mirror suspensions)
  - Get out of the rigid single sampling frequency operation (10 kHz) and move on a more performing and flexible multi-rate system
  - Further increase of locally available computation power to increase data quality analysis capabilities and properly assist control design and implementation mainly for the last stage of suspension and new payload

# UDSPT Board

- Result of design effort is a high performance signal conditioning, signal conversion and processing platform that enables users to implement state of the art hard real time control system. Board can be operated in standalone mode or in cooperation with other boards.
- Form factor is a variation of a Double Compact Module PICMG<sup>®</sup> AMC.0 R2.0 AdvancedMC module (variation consists in a wider board than what specified for a Double Module)
- The key features of the UDSPT board are:
  - Texas Instruments' multi-core DSP – TMS320C6678
  - 512 Mbytes of DDR3-1333 Memory
  - Two Gigabit Ethernet ports supporting 10/100/1000 Mbps data-rate
  - 170 pin B+ style AMC Interface containing SRIO and Gigabit Ethernet
  - IRIG-B input
  - Module Management Controller (MMC) for Intelligent Platform Management Interface (IPMI)
  - Powered by DC power-brick adaptor (12V/3.0A) or AMC Carrier backplane
  - Two on board FPGA: one Xilinx Spartan3 dedicated to processing unit and one Altera Cyclone IV interfacing data converters
  - 6 x 24b 3.84 MHz ADC converters
  - 3 x 24b 320 kHz DAC stereo converters (6 channels individually addressable)
  - Converters sampling frequency DSP IRQs synchronous with IRIG-B signal
  - Fully differential input channels and balanced output channels

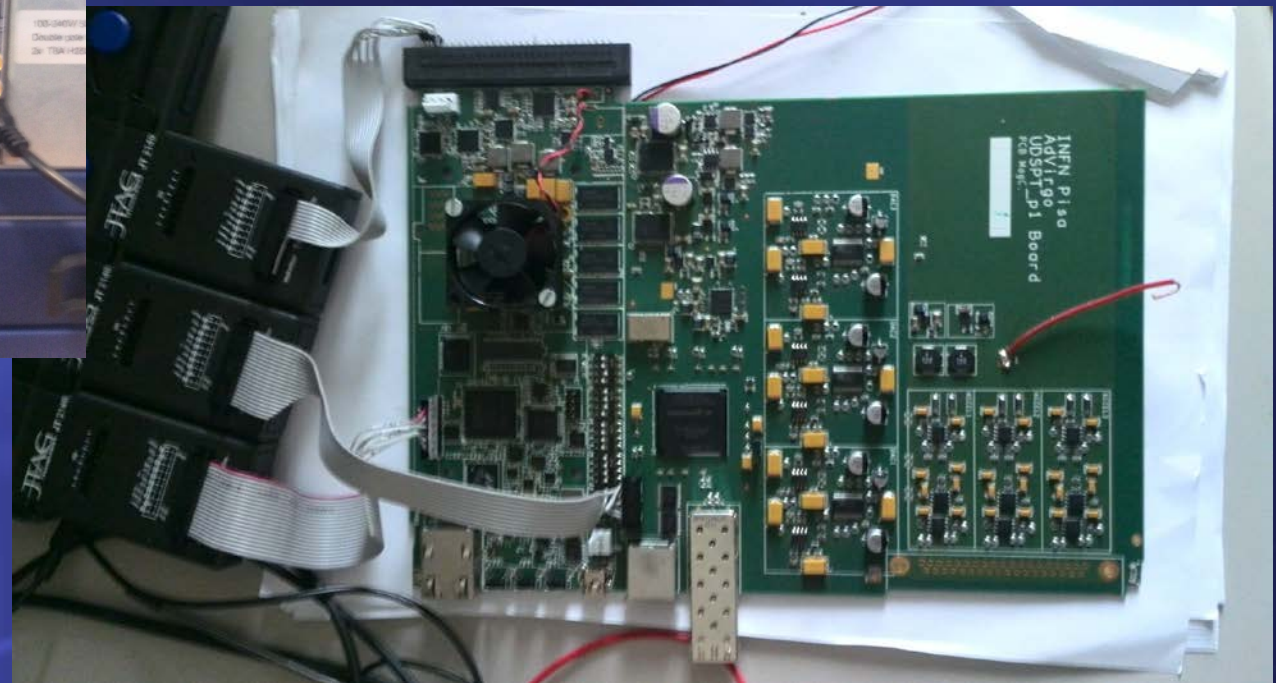
# UDSPT Board





# UDSPT Board

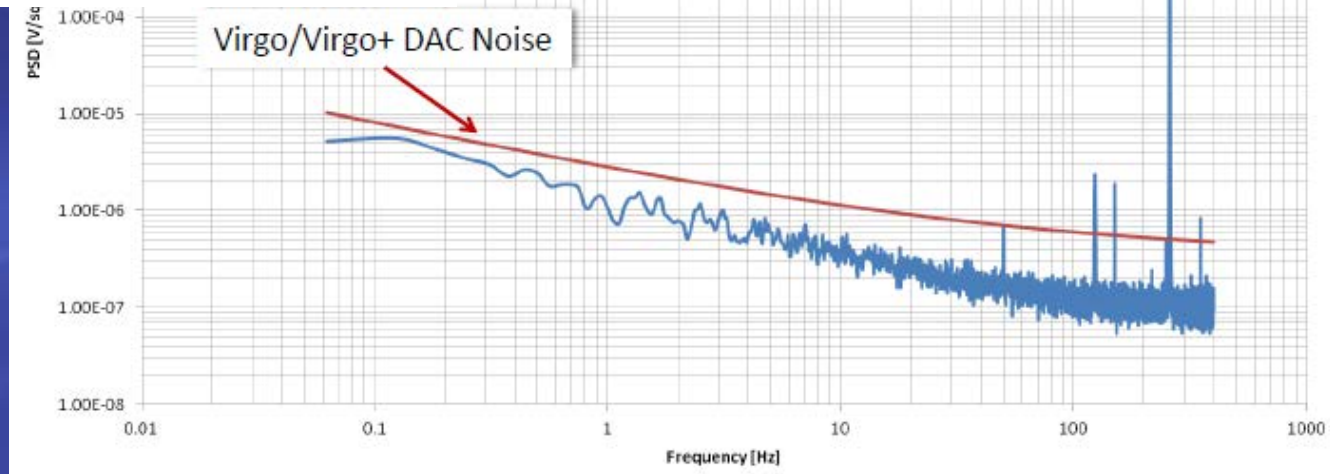
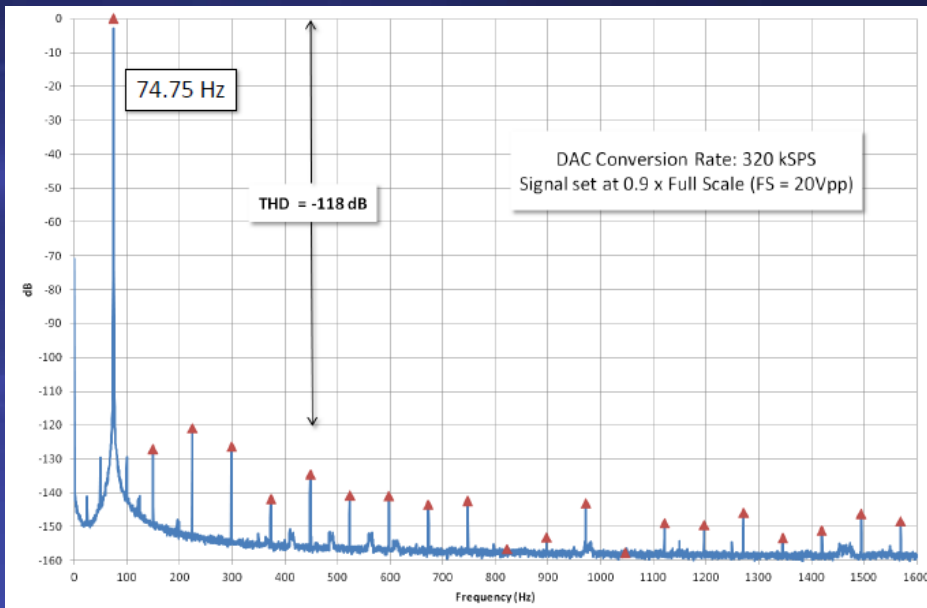
- Board complexity (250 different parts, a total of 2500 components) was compensated by a modular design. Processing, data converters and front-end occupy pre-defined areas. Strong effort in interfaces design



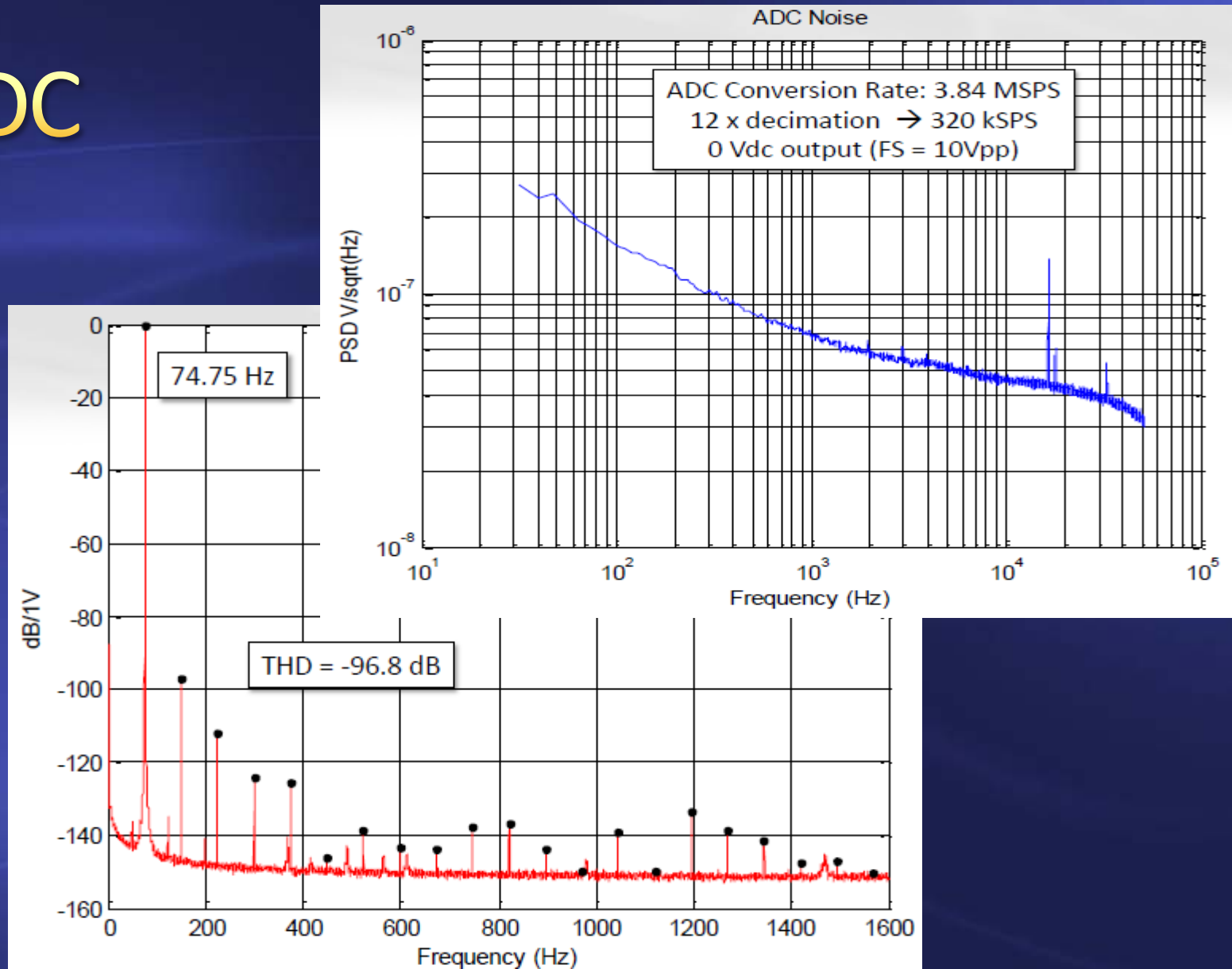
# Performances

- Digital I/O
  - Gb Ethernet (tested up to 30 MB/sec) System - Rest of The World communication
  - PCIe (tested up to 400 MB/sec) On Board Communication
  - SRIO (tested up to 1.6 GB/sec) Board-to-board communication
- DSP Software
  - Tested operation up to 320 kHz sampling rate (3.125 usec interrupt request repetition cycle)
  - Matrix( $n,m$ )\*Vector( $m,1$ ) double precision multiplication requires  $0.5*nm+n+m$  nanoseconds →
    - State space with 3 inputs, 3 outputs and 12 states requires less than 200 nsec

# DAC Performances

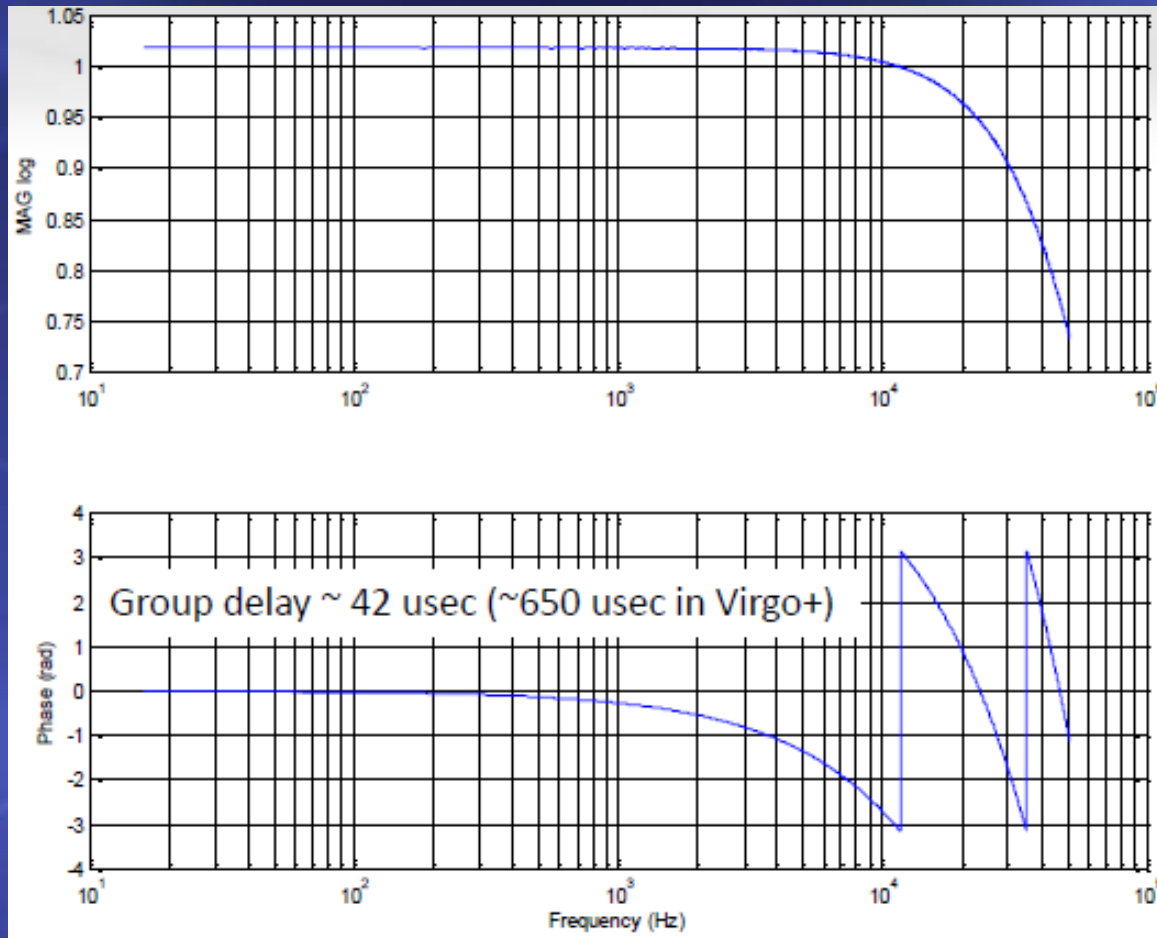


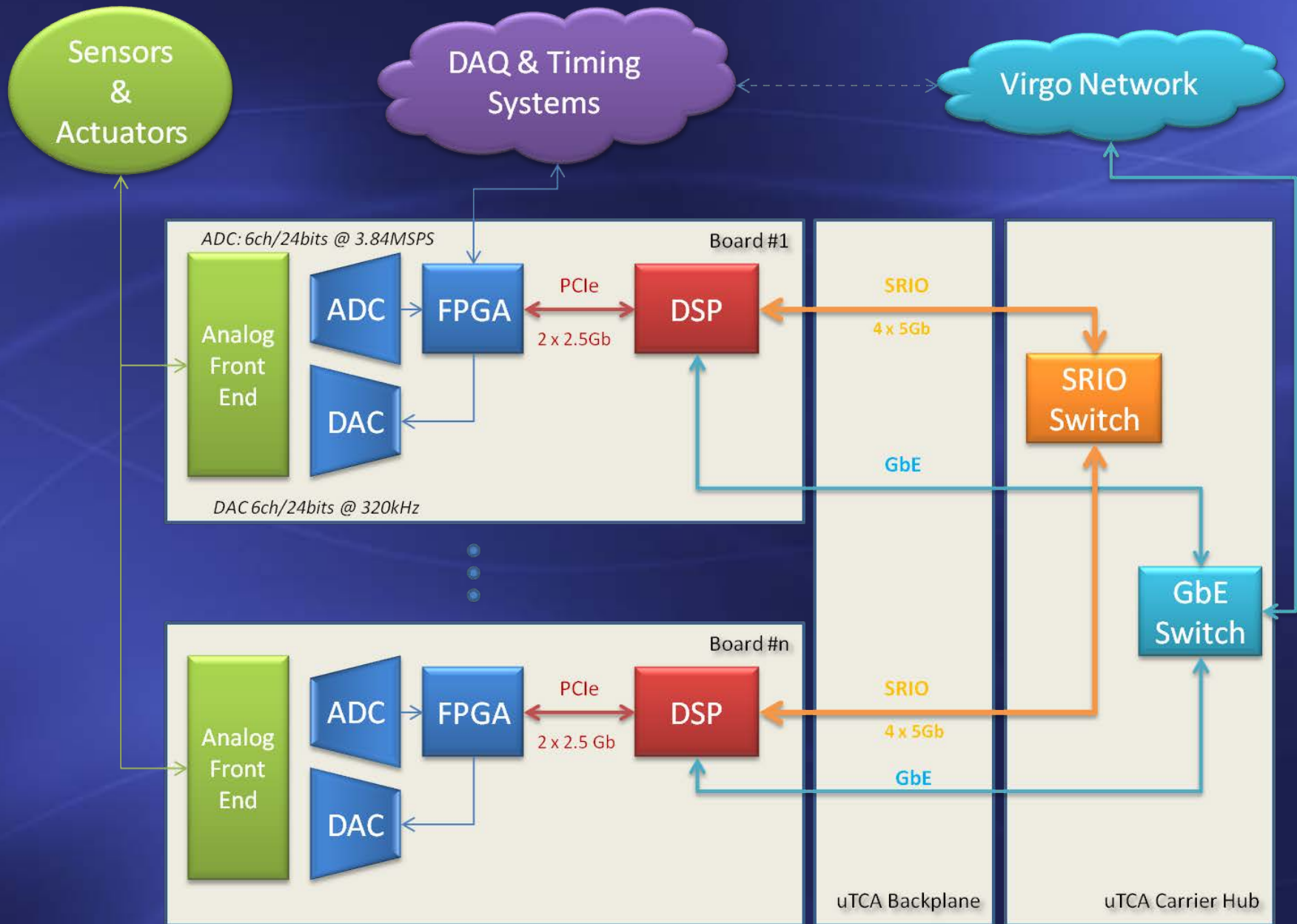
# ADC





# ADC-DSP-DAC Transfer Function





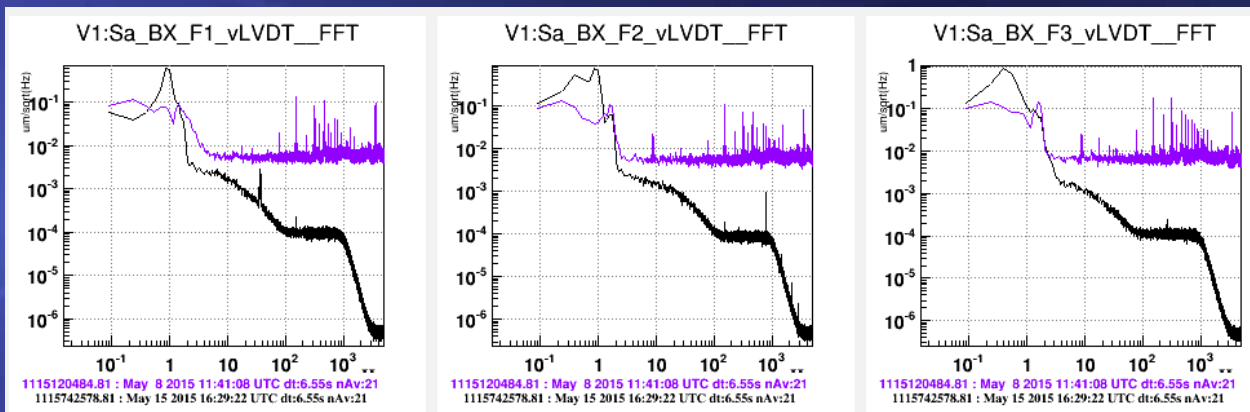
# Result:



In a single 6U x 19" crate we can concentrate 72 ADC + 72 DAC channels supported by 720 GFLOPs, 12 x 1 Gb Ethernet ports + 12 x 1 Gb Optical Link for digital IO and a total power consumption less than 500 Watts

# Performances: ADC Noise & EM Noise Immunity

- Performances tests on BS suspension went beyond our expectation. Placing converters at front-end electronics level, together with introduction of digital demodulation, drastically improved noise immunity. Following picture shows improvement in vertical position sensors readout.





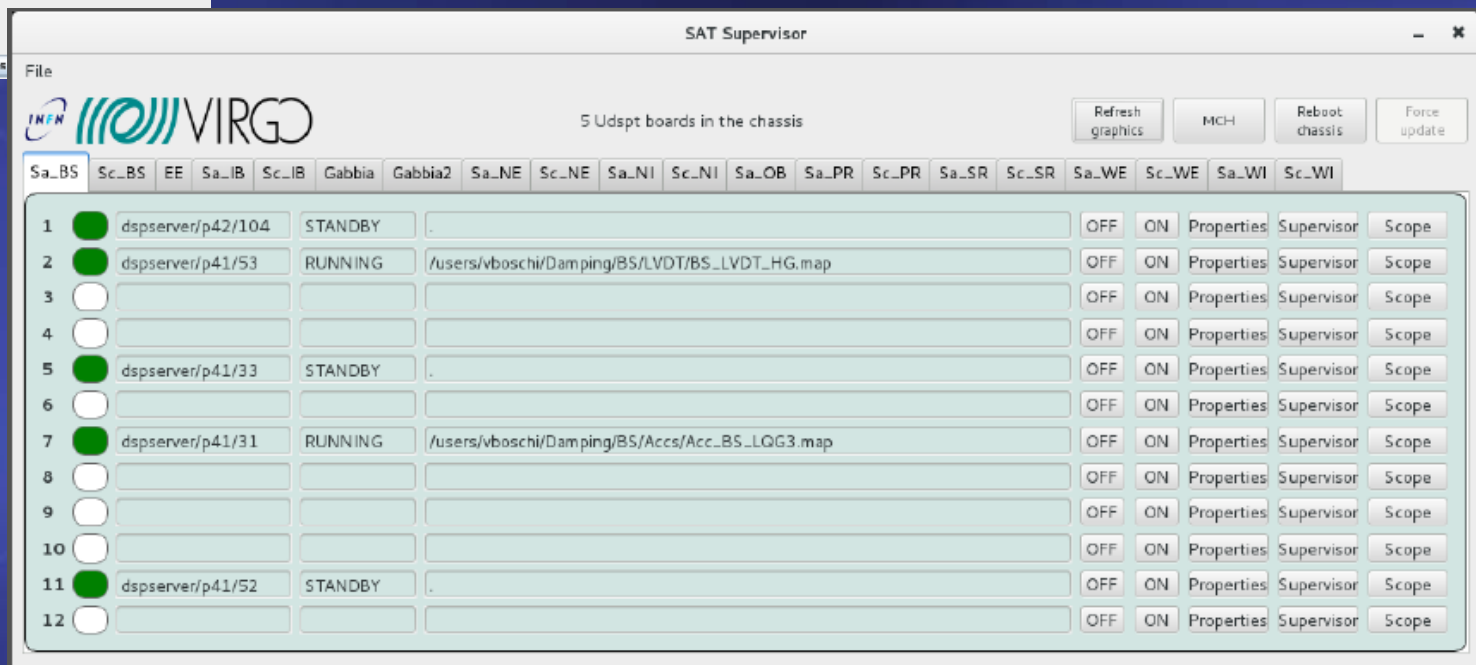
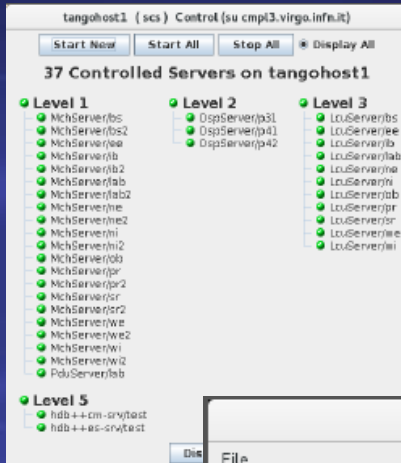
# Installation

- Board production was completed last July and installation is progressing fast. The following table summarizes installation status updated to July 28th.

	<i>BS</i>	<i>WI</i>	<i>NI</i>	<i>PR</i>	<i>SR</i>	<i>IB</i>	<i>OB</i>	<i>MC</i>	<i>WE</i>	<i>NE</i>	<i>BPS</i>	<i>Total</i>
<b>Total</b>	15	15	15	15	15	14	7	14	15	15	1	141
<b>Installed</b>	12	10	12	7	12	12	6	0	2	2	1	76
<b>To be installed</b>	4	5	9	8	3	2	1	14	13	13	0	65
<b>%</b>	73	67	40	47	80	86	86	0	13	13	100	54

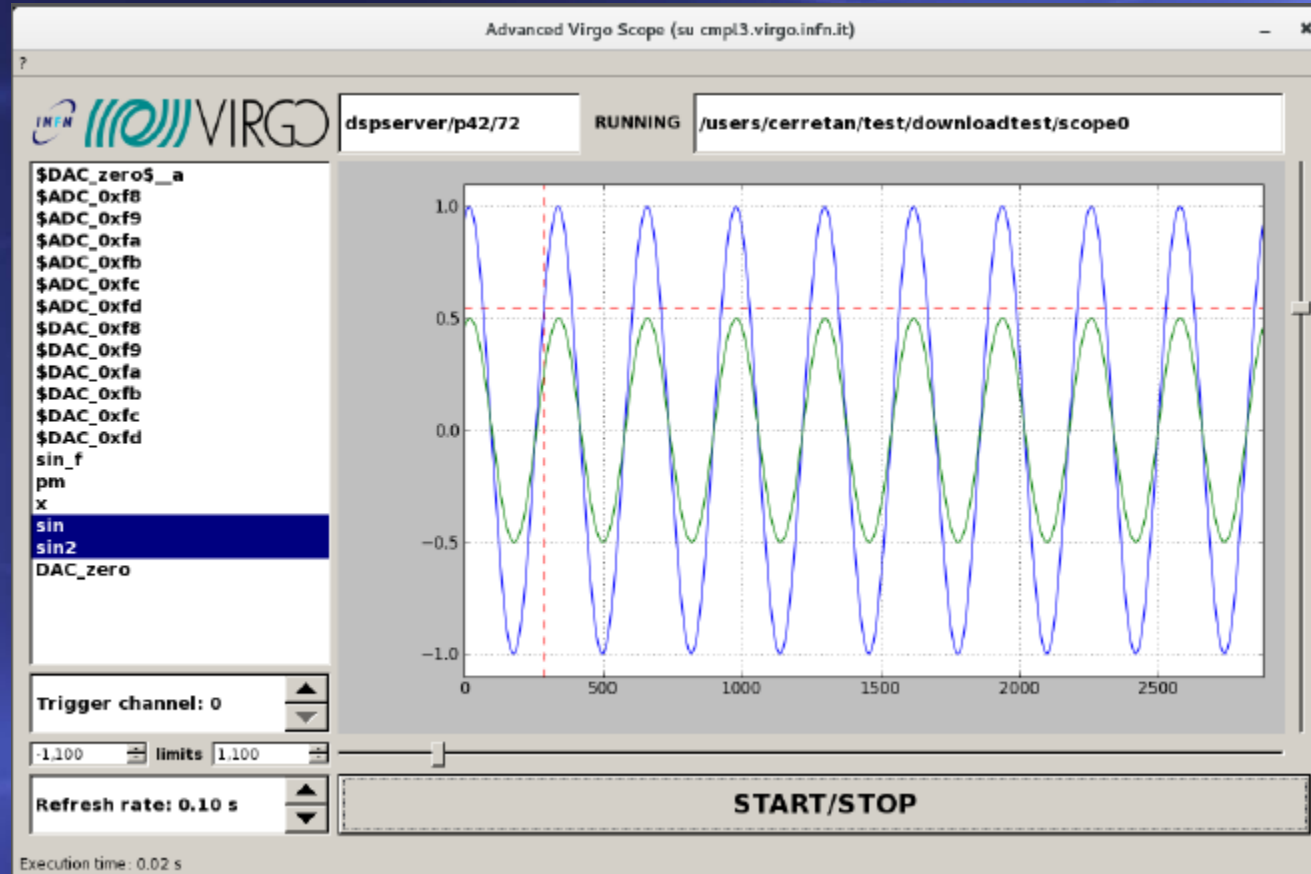
# Software Supervisor

- For initial AdV, software shall support about 150 boards. At system startup each board loads boot code via tft from a dedicated boot server. This code is actually a sort of basic OS. In a second phase software supervisor (tango-based) downloads in each processor the hard real-time code.



# Real Time Scope

A nice tool for system debugging is a real-time scope that can access any single variable declared into the source code. Work is in progress to provide real-time fft and few more functionalities



# Conclusions

- A new system to control suspensions and mirrors was developed and installation is almost completed.
- Still some work in progress on software side and, as usual, will almost never end
- Extensive use of supervising software, mysql databases and third parties tools will simplify operation and maintenance

