CIRCUIT DESIGN OF THE VIRGO+ FILTERING MEZZANINE.

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ABSTRACT:

The filtering mezzanine, which is described here, is an electronic developed for the VIRGO experiment. It takes place in the VIRGO+ electronics development, an involved acquisition system. This electronic module is able to make a compression filtering and an anti-alias filtering for the analog to digital conversion in a full differential solution.

The compression part performs two 2^{nd} order filters allowing the gain to increase with a ratio ~35 between two selectable frequencies.

The anti-alias part performs a Butterworth 6^{th} order filter.

Because of the high number of channels foreseen, we implemented this analog module in a mezzanine version which allows to tune easily the compression and anti-alias parameters. Each mezzanine can be identified with its proper parameters thanks to an EEPROM.

CONTENTS:

1- Introduction: principle and general description of the *VIRGO+ filtering mezzanine*.

The filtering module is composed of a first stage which performs a compression filtering and of a second which performs an anti-alias filtering for the following ADC. It is plugged on the acquisition board.

Its first aim is to adapt the input analog signals coming from several other systems. Because of the necessary compliance between systems and because of an essential electronic immunity (especially in mixed signals operations), we decided to implement the full chain in a differential mode: from the input cable to the ADC.

Compression filter:

The compression filter transfer function is the same than the already existing compression filter: using two poles and two zeros, we increase the gain from 1 to ~35 between two cut-off frequencies.

These frequencies can be tuned by the choice of appropriated components. We kept the possibility to bypass the compression by the use of 0Ω straps. The gains before/after the compression are ¼ - 9 to fit to the adc input dynamic range. For cost and consumption reasons, a type of mezzanines have been implemented without the input compression filter.

Anti-alias filter:

The anti-alias filter is a 6^{th} order Butterworth type.
We chose this type of filter because of its stability before the cut-off frequency and because of its constant delay.

The chosen ADC is an 800Ksps/16bits. So, to preserve the low-frequency band (0-10kHz) - which is the most important for the photodiodes channels - we have to cut-off the full ADC input dynamic before the Shannon frequency (the half sampling frequency → 400kHz).

The signals frequency bandwidth is DC-100kHz.
We decided to implement a 6^{th} order filter with Fc=100kHz.
At first, we added two notches centered at the Shannon frequency to finally reject the remained dynamic range. Finally we will see that it turned out to be not used because of 50Hz EMC problems.

This solution allows to use a limited number of electronic stages and so a limited number of components because the size, the delay and the power consumption were important specifications.

Two series have been produced between 2007 and 2010. The use of the first production on site has allowed to identify different problems as 50Hz or glitches.

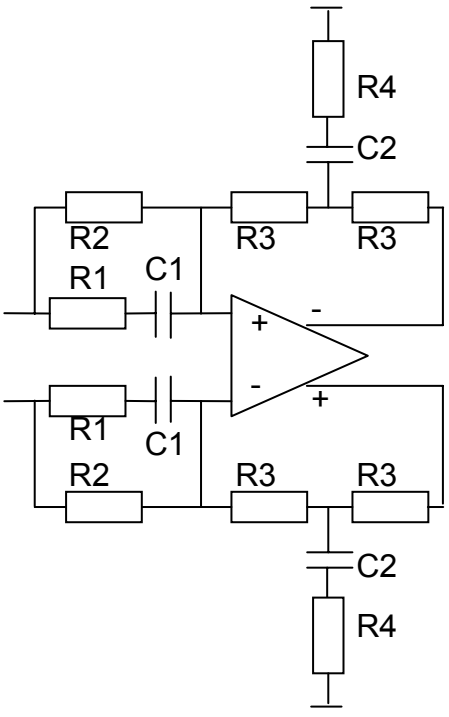
2- Technical description and solutions.

The two filters are performed using the same amplifier: ***OPA1632***.

We chose this component because of its low-noise, its full-differential architecture and its bandwidth: 1,3nV/√Hz (7nV/√Hz at 10Hz); BW=180MHz; SR=50V/µs. An important issue is the 1/f cut off frequency. OPA1632 is a rare and good differential amplifier which can cover the frequency range.

2-1 Compression filter:

The compression filter architecture is full differential.
Its shape is performed using two merged zeros and two merged poles.
The cut-off frequencies can be tuned choosing the component as follows:



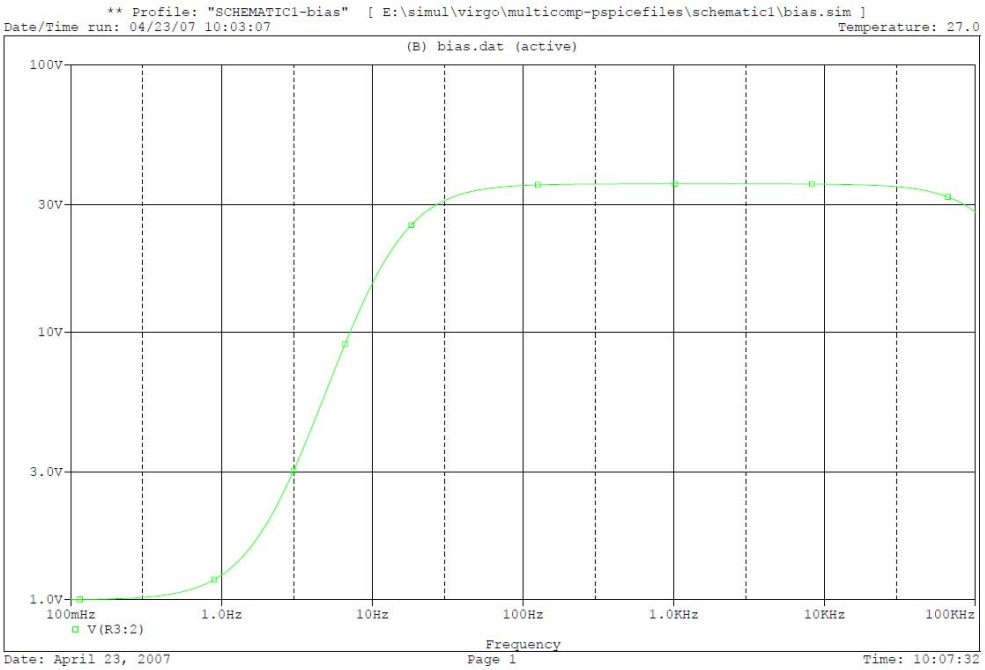
$$fp_1 = \frac{1}{2\pi R_1 C_1}$$

$$fp_2 = \frac{1}{2\pi R_4 C_2}$$

$$fz_1 = \frac{1}{2\pi(R_1 + R_2)}$$

$$fz_2 = \frac{1}{2\pi(R_4 + R_3/2)}$$

Following, the transfer function of the compression filter for 2Hz-12Hz filtering. Gain unit is normalized to 1 in the low frequencies domain. To fit to the ADC input dynamic range, the gains are ¼ to 9 before and after the cut-off frequencies.



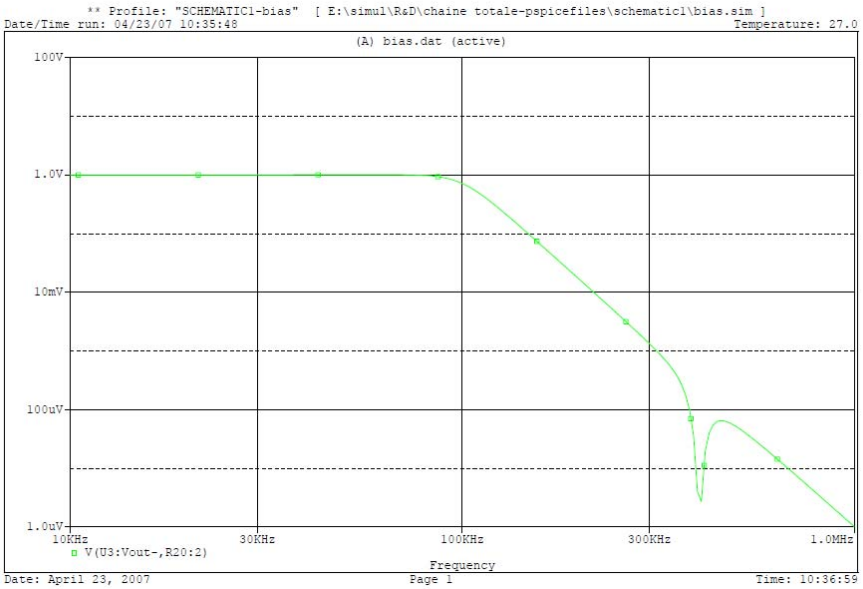
2-2 Antialias filter:

The foreseen ADC dynamic range is 18bits, so ~17bits real. As it corresponds to a ~100dB dynamic, we should have this dynamic attenuation at the half sampling frequency (Shannon freq.).

The chosen ADC (AD7674) is a 800Ksps, so the Shannon frequency is 400kHz. The desired bandwidth is ***100kHz*** for interferometer control issues.

The full dynamic attenuation should require to implement a 10^{th} order filter. Due to specification considerations as delay or number of components, we decided to implement a 6^{th} order filter with three 2^{nd} order cells. Two notches can be added. By default, notches are not implemented.

Following, the transfer function with 400MHz double notch.



On the differential amplifier used, a Vocm pin allows to shift the two outputs DC common mode voltages. For the 0-5V input range ADC, it will be very useful to shift this common mode voltage to the half of the input range (+2,5V).

Principle of the Butterworth 6th order filter:

This filter is implemented with three second order stages.
For a Butterworth type, we need to have quality factors about:
1,92 ; ***0,7*** and ***0,518*** for the different stages.

The quality factor can be written as:

$$Q = \frac{\sqrt{2mn}}{1 + m(1 - K)} \quad \text{and} \quad fc = \frac{1}{2\pi R_2 C_1 \sqrt{2mn}}$$

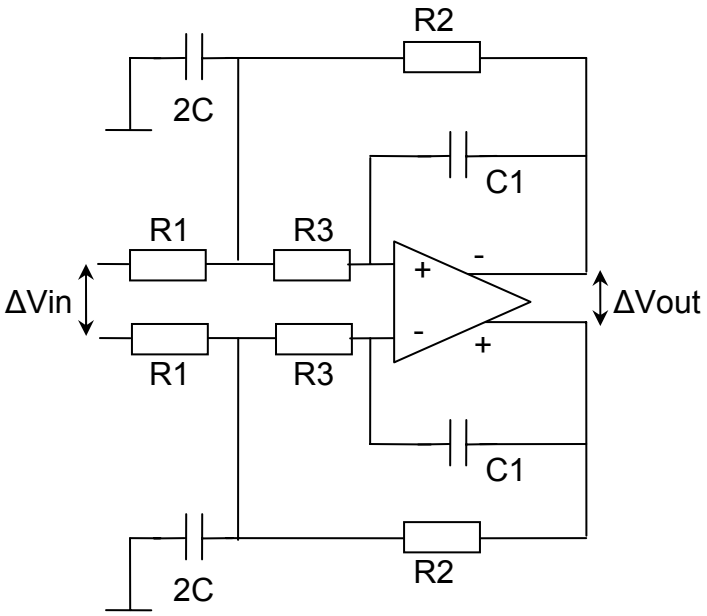
With K the normalized low frequency gain ***K= -1***, and ***m=R3/R2***; ***n=C2/C1***.

With ***R1=R2=R3=500Ω***, ***m=1***,

$$Q = \frac{\sqrt{2n}}{3} \quad \text{and} \quad fc = \frac{1}{2\pi R_2 C_1 \sqrt{2n}}$$

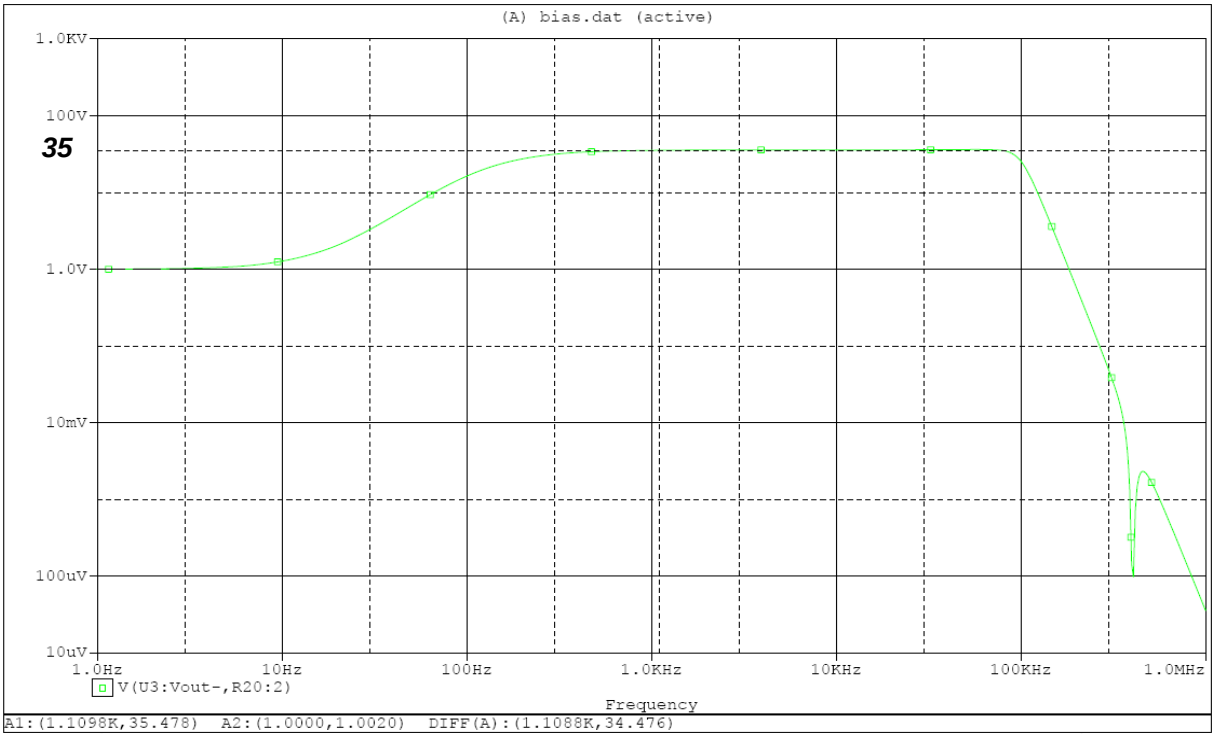
For ***Q=0,518*** ; ***n=1,21 → C1=683pF*** and ***2C2=1,65nF***
For ***Q=0,7*** ; ***n=2,2 → C1=500pF*** and ***2C2=2,2nF***
For ***Q=1,92*** ; ***n=16,8 → C1=183pF*** and ***2C2=6,15nF***

The different stages have to be cascaded with increasing Q factor to avoid electronic saturation.



Full chain simulation: compression & anti-alias transfer function.

Here Fz=20Hz and Fp=120Hz. Implementation of 400MHz double notch.
Gains are normalized to 1 for the low frequencies domain.

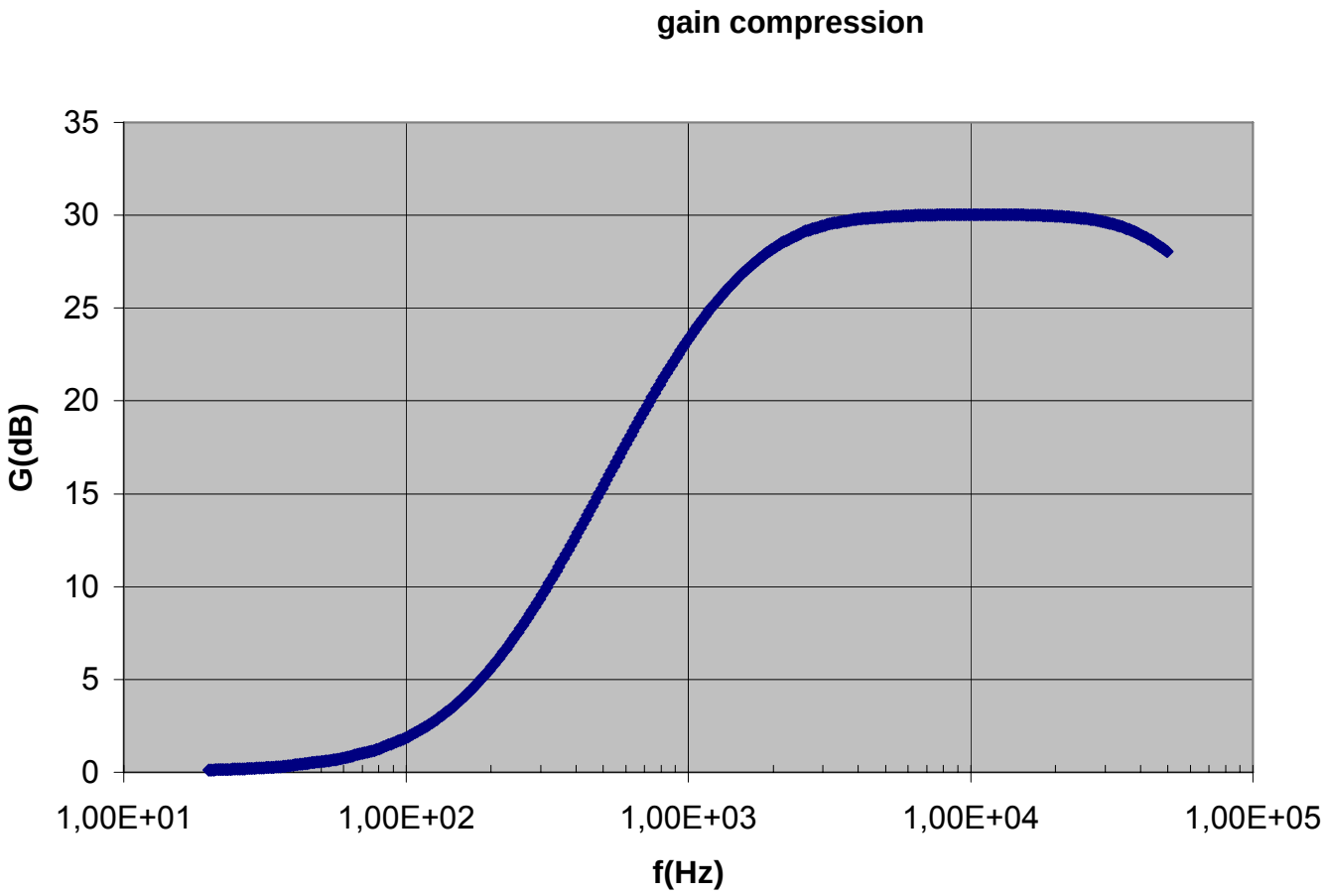


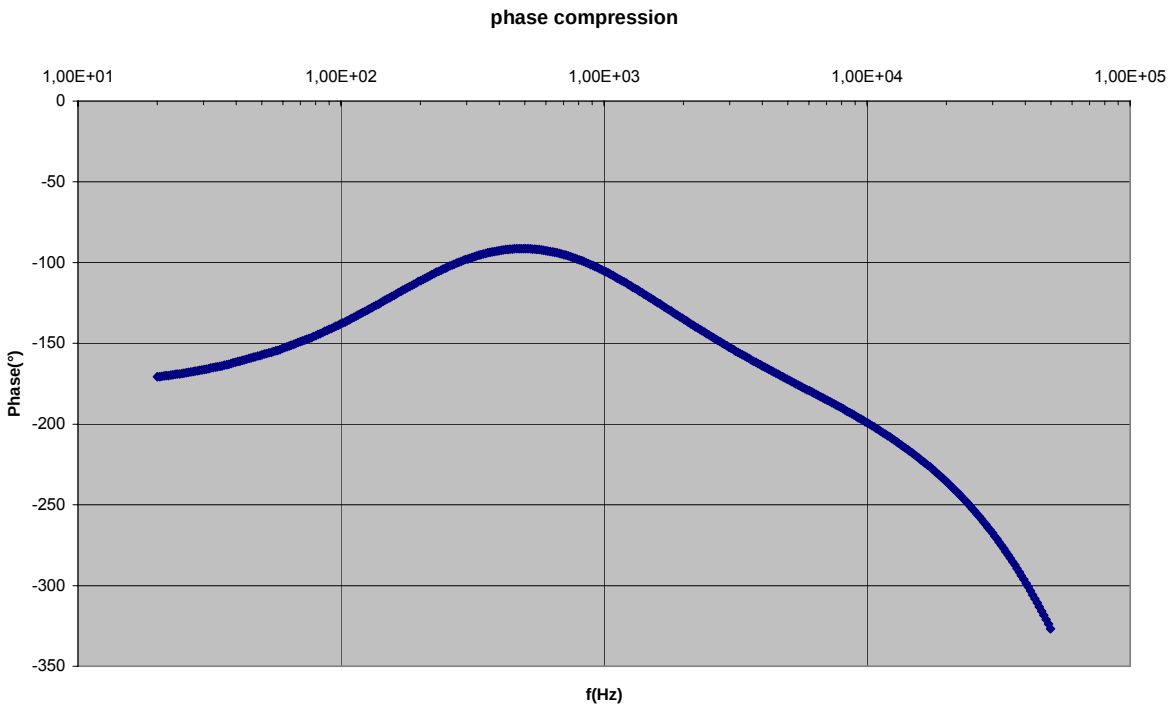
3- *Tests & finalising.*

In order to test the mezzanine, we developed a test board which performs a single-ended to differential conversion for the input signals (OPA1632) and a differential to single-ended conversion for the output signals (AD8130)-(see appendix).

- ***Compression***

We performed transfer functions using a frequency analyser.
Here, Fz=200Hz and Fp=1200Hz.

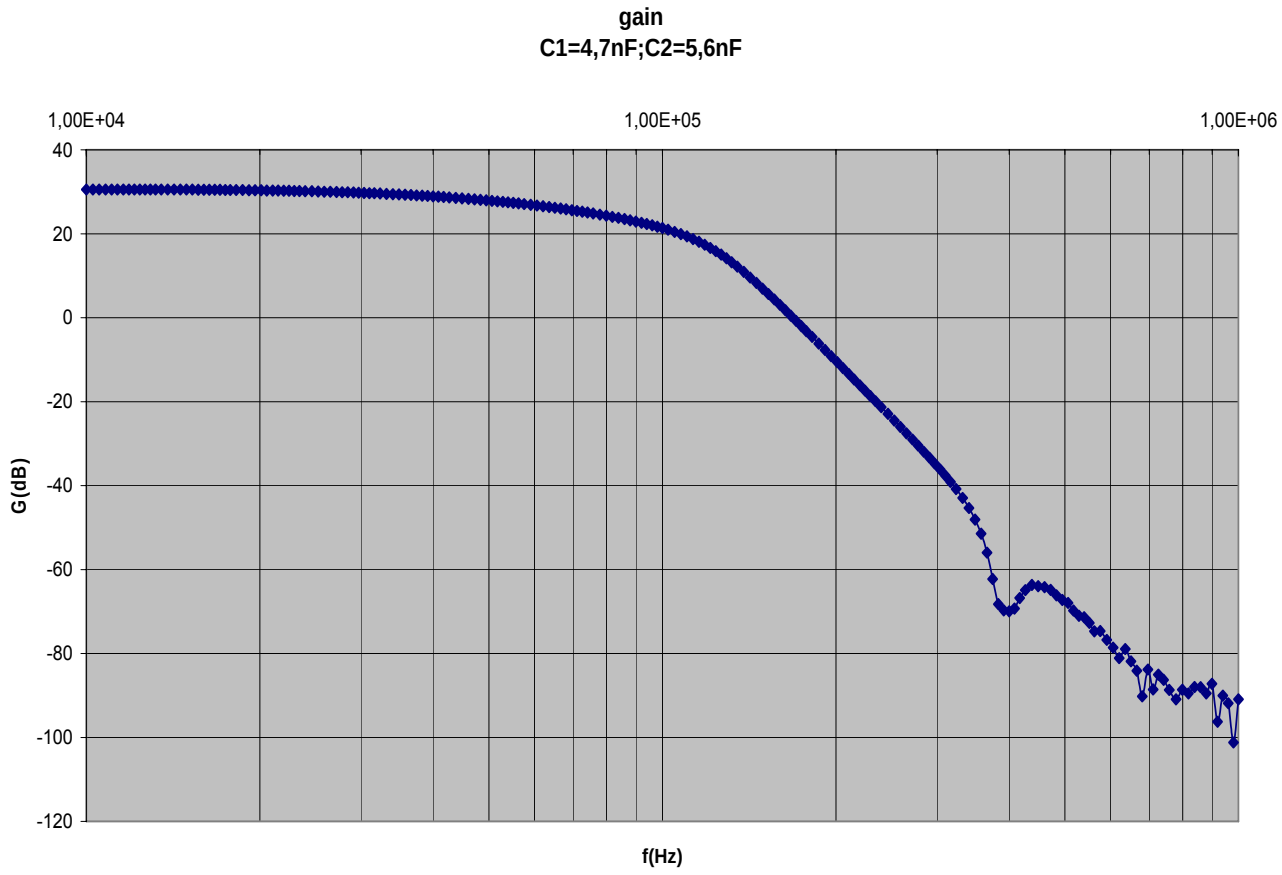



phase compression
1,00E+01
1,00E+02
1,00E+03
1,00E+04
1,00E+05
0
-50
-100
-150
-200
-250
-300
-350
Phase(°)
f(Hz)

- ***Anti-alias***

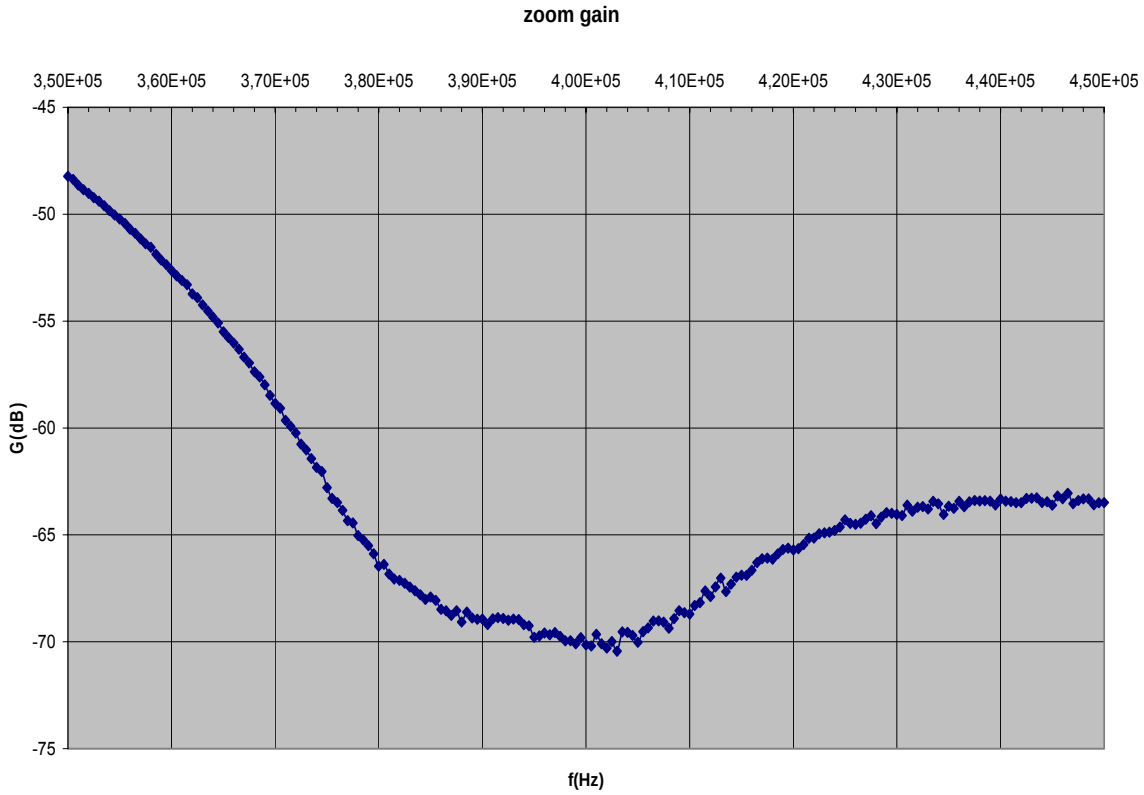
Because of the difficulty to tune perfectly the two notches at a fixed frequency (400kHz), when used, we lightly shift the two frequencies: one below and one above.

Transfer function with compression and two tuned notches:
C1 & C2 the two notches capacitances (L=33µH).

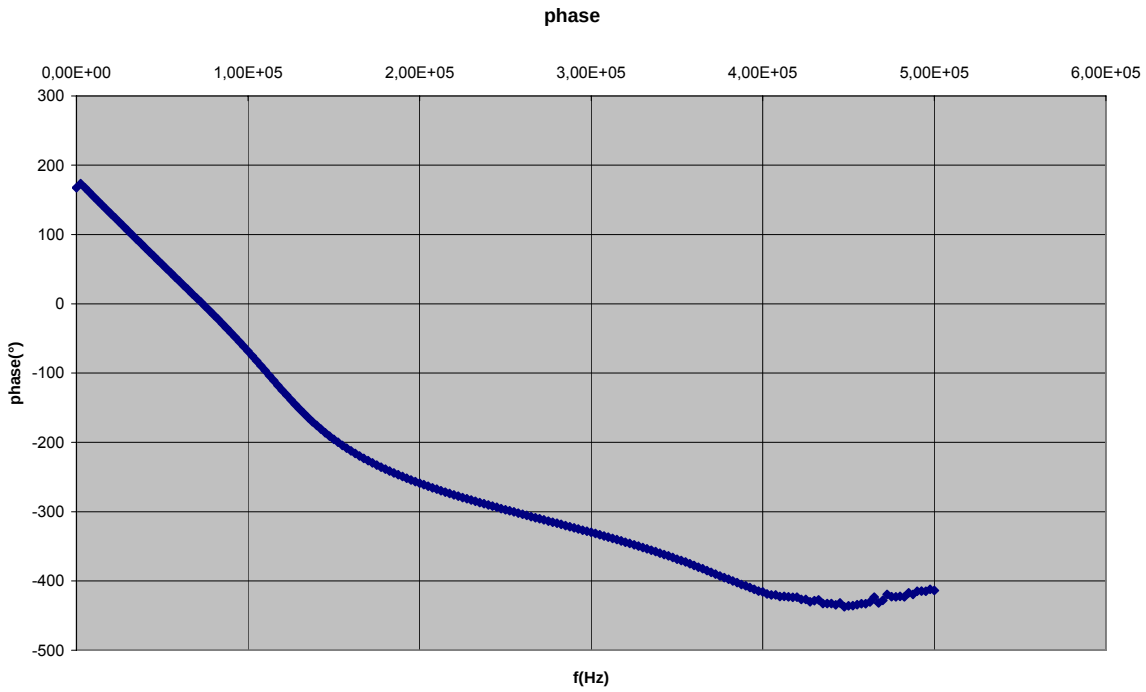


The low frequency gain is 30dB because we used the compression input stage with a 30dB gain in order to cover the analyzer dynamic range. The cut-off frequency is 100kHz (g=-3dB). At the Shannon frequency the gain is -70dB which represents a -100dB rejection with the use of notches. With not, the rejection is about -90dB.

Zoom of the notch attenuation, width:



Phase of the filter: DELAY



As the phase decreases linearly with the frequency, the delay of the filter is constant and is about ***6,8µs*** before the cut-off frequency.
Of course this delay does not include the compression inversion (-180°).

- ***<u>First production feedback:</u>***

A first production allowed to test and to identify problems on long term use.

We identified a 50Hz perturbation introduced by the notches. So we decided to remove them.

We noticed a variable frequency line. We identified a problem of stability on one of the stages of the anti-alias. We solved the problem adding capacitors in parallel on the feedback resistances. These capacitors can be mounted over the resistances.

We noticed a problem of linearity introduced by a step in the ADC output code. We think it is due to a problem of charge injection and decoupling between the amplifiers and ADC. Tests have not allowed to understand definitively the problem but it has been reduced in acceptable tolerance using a capacitor at the differential output of the mezzanine. It acts as a charge reservoir. The use of this capacitor should limit the available output current and so the high dynamic ranges for high frequencies signals. As this effect is possible for frequencies over 10kHz, signals should not be affected.

These modifications have been done on both productions.

4- *Tuning & identification.*

4-1 Tuning:

Compression filter cut-off frequencies and gains are fixed using capacitances and resistances.
The gains before zeros and after poles are fixed by resistances, so only capacitance should tune the cut-off frequencies. As cut-off frequencies are quite low (several Hz), we limit to 10µF the capacitances and so make vary the resistances. To fit to the ADC input dynamic range, the gains are ¼ to 9 before and after the cut-off frequencies.

Finally 4 sets of filters have been produced:

- No compression: 1st OPA removed; C30=C31=1,5kΩ; R2=R3=0Ω.
- 2Hz-12Hz compression: C1=C2=470nF; C3=C4=10µF; R1=R4=24kΩ; R2=R3=120kΩ; R5=R6=R10=R11=15kΩ; R7=R8=1,5kΩ.
- 4Hz-24Hz compression: C1=C2=680nF; C3=C4=10µF; R1=R4=10kΩ; R2=R3=51kΩ; R5=R6=R10=R11=6,8kΩ; R7=R8=680Ω.
- 10Hz-60Hz compression: C1=C2=680nF; C3=C4=10µF; R1=R4=4,3kΩ; R2=R3=21kΩ; R5=R6=R10=R11=2,7kΩ; R7=R8=270Ω.

To avoid the compression filter and so have an inverter function, we implemented solder pads for 0Ω resistances (straps).
They are referenced as R9, R30, R31 and R32.

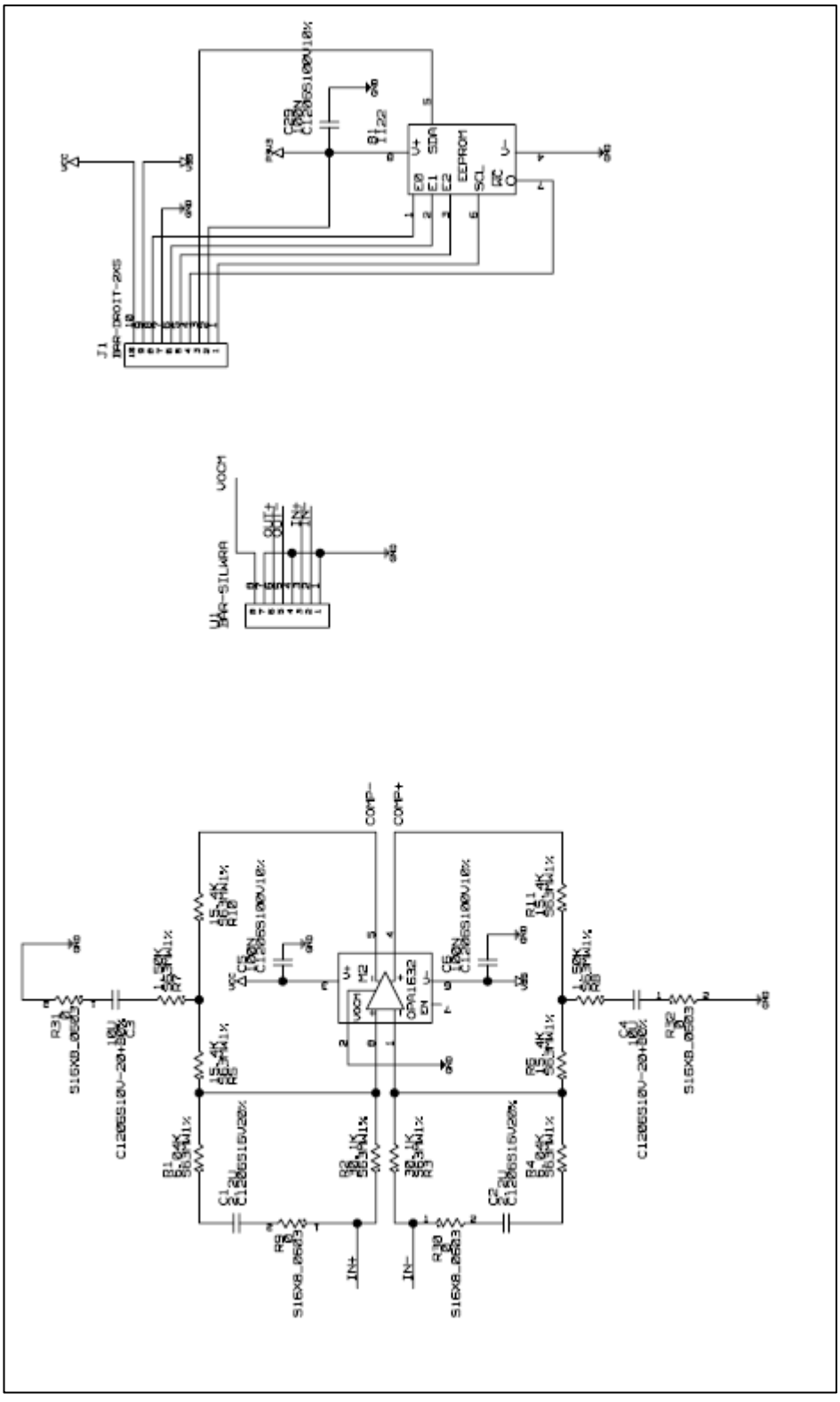
4-2 Identification:

The final foresaw number of acquisition channels is about 1400.
So we need to access the information concerning the filters directly on the mezzanine, as serial number, cut-off frequencies, notches, particularities, location...
We implemented a 256 byte I2C EEPROM which allows to save 256 ASCII characters.

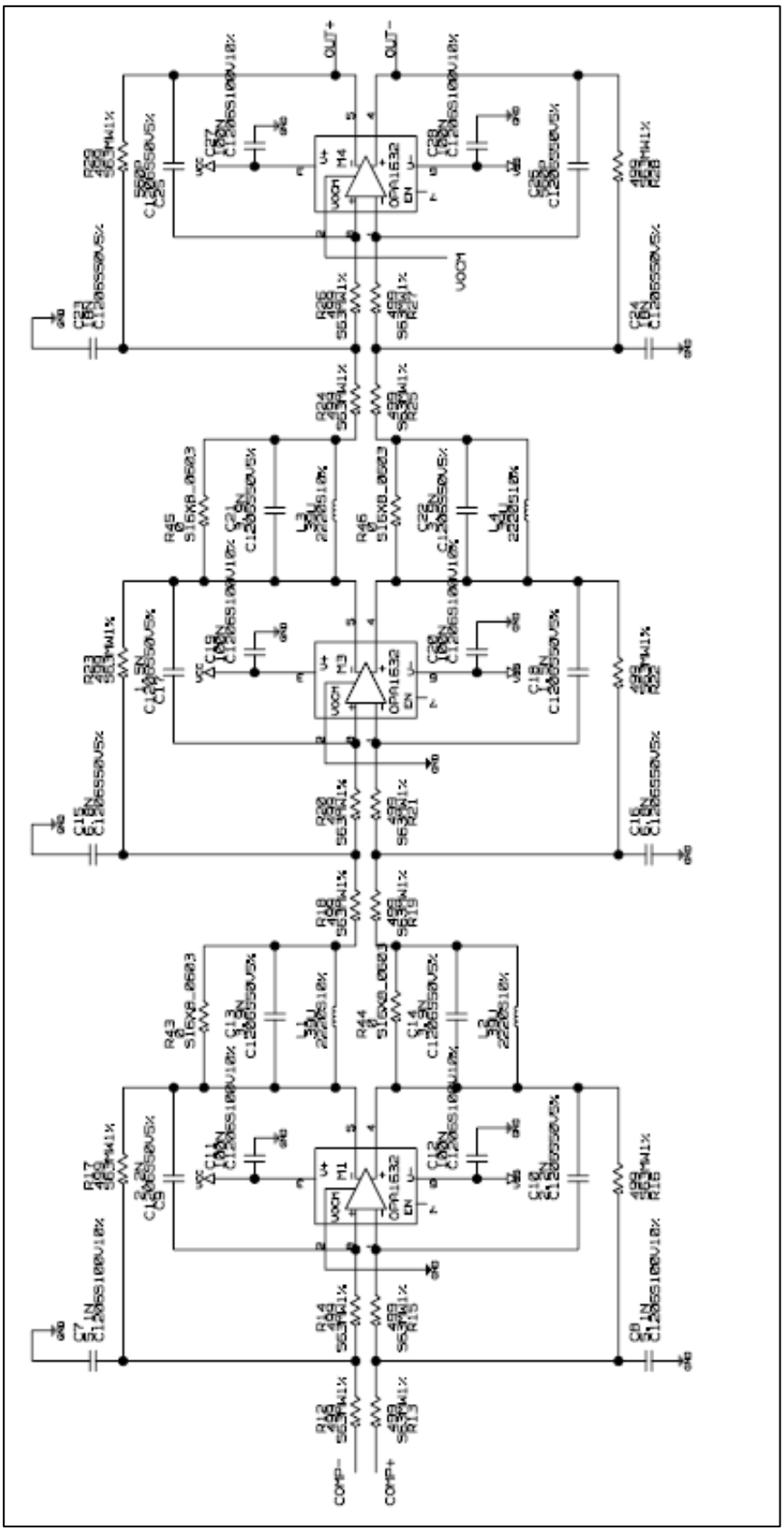
We access this EEPROM directly by the acquisition board or by the test/programming system.

APPENDIX:

compression/EEPROM/connectors schematics.

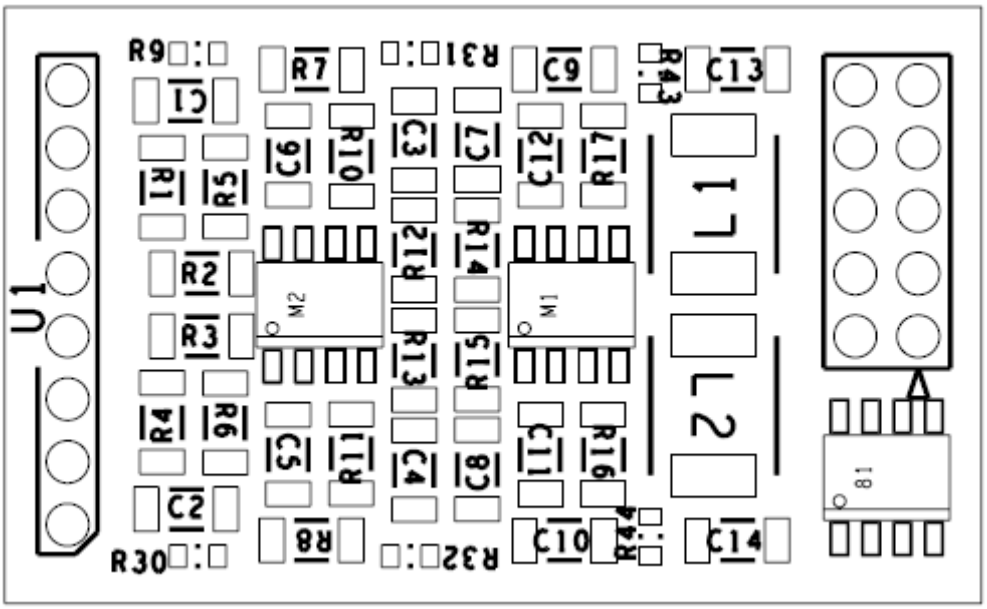


Anti-Alias schematics.

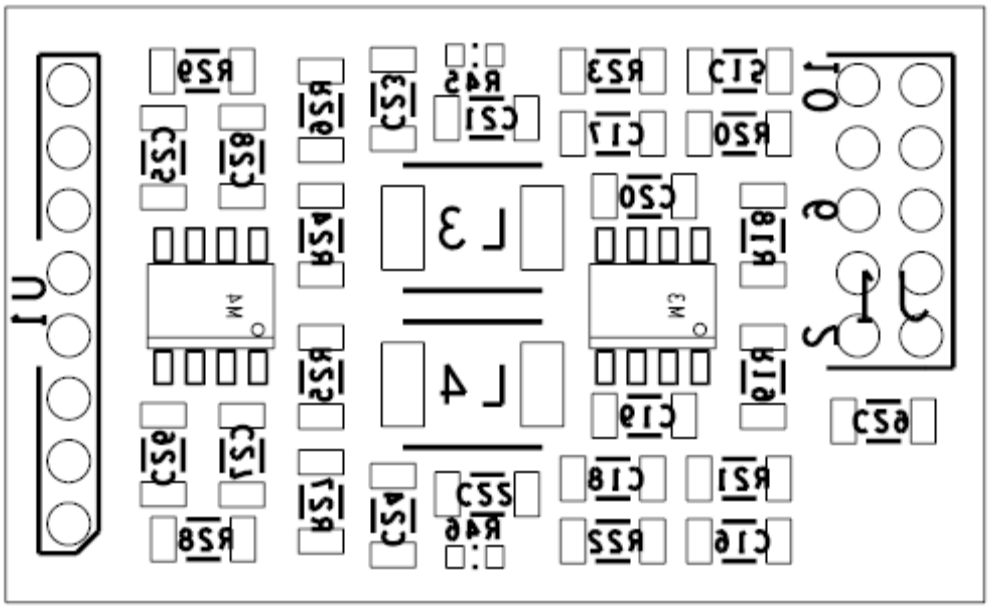


Layouts

TOP



BOTTOM



Tests board schematics.