Adv Virgo SAT Electronics Availability

A. Gennai for
Suspension Control System Group

Introduction

- The SCS Group is in charge of SAT (and PAY and partially INJ) control
- At present about 7 FTE and 1 PhD student are fully involved in system development
- It is worth reminding that according to our experience hardware development represents no more than 20% of total work that is by far dominated by software development, controllers implementation, debugging, fine tuning, noise hunting, maintenance, …
  - Old system was developed in a couple of years but then it has been operated for 16 years. Even adding the time spent for development of new version of DSP and Coil Drivers the time devoted to hardware production is still below 20%

New Boards Status

- Components Procurement
  - Active Components already available for whole production
- Passive Components
  - Provided by firm in charge of boards assembly (order in next hours)
- Boards Production
  - 4 boards(ACC) already available and fully tested (see contributions to last 2-3 weekly meetings)
  - 20 PCBs(LVDT) already delivered
  - First two assembled boards will be delivered on Feb 16th
  - Remaining boards supposed to be delivered within Feb 20th
- Budget
  - Already committed about 70% of SAT Control System budget
  - Remaining 30% is for PCB production and assembly.

SCS Boards – Needs

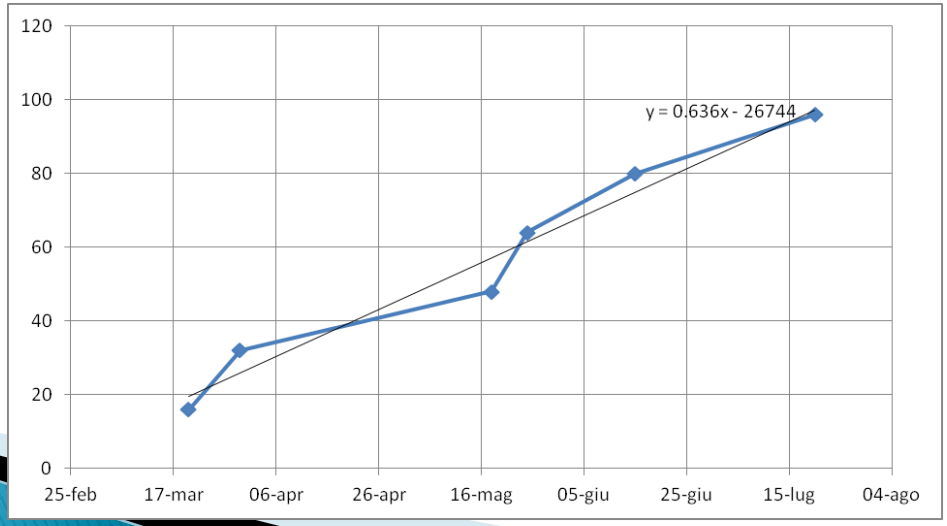
Part	Accel	Lvdt	Coil Drv
Base Ring		1	
Top Stage	2	1	1 (HP)
Fishing Rods		1	
Total LCU Top	**2**	**3**	**1**
Steering Filter		1	2 (HP+LN)
Payload		3	4 (HP+LN)
Total LCU Bottom	**0**	**4**	**6**
Total	**2**	**7**	**7**

BS susp

- Accel: 3 ch/brd
- Lvdt: 6 ch/brd
- CD: 6 ch/brd (HP) or 3 ch/brd (HP+LN)

Following SAT schedule ...

Task	Date	Acc	Lvdt	CD	Total
WI Integration	**20-mar**	2	7	7	**16**
NI Integration	**30-mar**	4	14	14	**32**
PR Integration	**18-mag**	6	21	21	**48**
SR Integration	**25-mag**	8	28	28	**64**
NE Integration	**15-giu**	10	35	35	**80**
WE Integration	**20-lug**	12	42	42	**96**

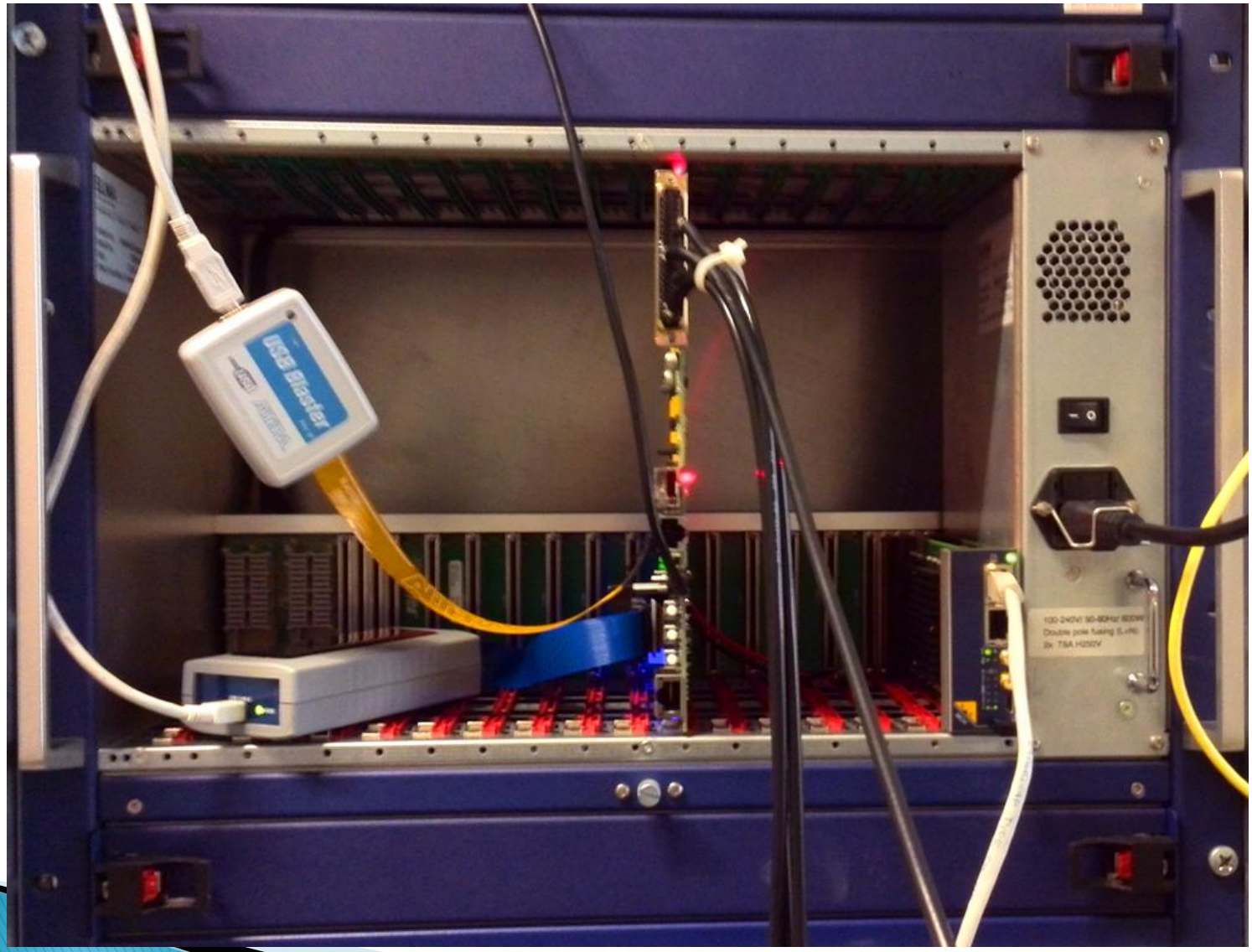


Boards Production

Task	Date	Acc	Lvdt	CD	Total	Available
P3 (LVDT) Released	**05-mar**					20
WI Integration	**20-mar**	2	7	7	**16**	
NI Integration	**30-mar**	4	14	14	**32**	
P4 (LVDT) Released	**08-mag**					100
PR Integration	**18-mag**	6	21	21	**48**	
SR Integration	**25-mag**	8	28	28	**64**	
NE Integration	**15-giu**	10	35	35	**80**	
WE Integration	**20-lug**	12	42	42	**96**	
P5 (CD) Released	**24-lug**					120

- A 6 ch. LVDT board can be used as Accel board (3 ch.) or as HP Coil Driver board with max 200 mA peak-to-peak output current (~ ½ max current we could drive into payload coils without damage)

microTCA chassis and new board test



Conclusions

- Electronics construction phase is rapidly converging to conclusion
- SAT installation and integration schedule (January 28th 2015 version) is compatible with electronics delivery schedule
- Still some concerns related to the lack of a laboratory (but Virgo site is so large that we will find some place to occupy temporarily)