

Phase noise requirements for the digital demodulation ADC clock of the AdV photodiode readout

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VIR-0208A-13 May 9, 2013

Summary

1	INTRODUCTION	2
2	PHASE NOISE COUPLING TO DEMODULATED SIGNALS	3
3	PHASE NOISE MEASUREMENTS WITH THE DEMODULATION TEST BOARD	4
4	PHASE NOISE PROJECTIONS ON THE TESTS RESULTS (8MHZ DATA)	5
5	SPECIFICATIONS ON THE PHASE NOISE	6
	 5.1 LOW FREQUENCY REQUIREMENT	6 6

1 Introduction

A noise cleaner provides the clock signal used for the demodulation ADC (see note VIR-0476A-12). Its purpose is to reduce the impact of the clock phase noise on the measurement, which is critical at high frequency since the digitization of a loud perfectly stable high frequency line will produce wide band noise if there is some ADC phase noise. Furthermore, once we demodulate the signal, the low frequency part of the phase noise couples directly to the demodulated signal.

The purpose of this note is to compute the requirement on this phase noise.

One may think to acquire also the reference signal of the modulation to monitor its phase noise and subtract it. Then the requirement will be on the relative phase noise of the two ADC channels used which usually will be located in the same DAQbox. If they are on distant DAQbox, then this requirement applies also on the system used to transport the phase information from one DAQbox to the next one (usually the timing system or a specific signal).

An appealing option is to extract the phase information from the channel itself using the signal at twice (or more) the modulation frequency as described in VIR-0476A-12.In this case, we nevertheless want to check this technique by comparing the signals obtained on different beams or by monitoring the modulation signal which means that anyway, we want that the phase noise requirement derived in this note applies within a DAQbox.

2 Phase noise coupling to demodulated signals

Let's assume that the input signal on the ADC is just a perfect sine wave with pulsation:

Then the input signal is:

$$Input(t) = Asin(\omega_{Mod}t)$$

 $\omega_{Mod} = 2\pi f_{Mod}$

Due to the phase noise, the ADC will sample this input signal with a time jitter $\Delta t(t)$

$$ADC(t) = Asin(\omega_{Mod}(t + \Delta t(t)))$$

$$ADC(t) = A\sin(\omega_{Mod}t)\cos(\omega_{Mod}\Delta t(t)) + A\cos(\omega_{Mod}t)\sin(\omega_{Mod}\Delta t(t))$$

Since the time jitter $\Delta t(t)$ is small we have:

 $ADC(t) = A\sin(\omega_{Mod}t) - A\omega_{Mod}\Delta t(t)\cos(\omega_{Mod}t)$

After demodulation by a sine wave at the modulation frequency $(\sin(\omega_{Mod}t))$ and low pass filtering, we are recovering the in-phase signal (dropping the factor $< \cos^2 >= 1/2$):

$$ADC_P(t) = A$$

By demodulating with a cosine, we get a none zero noise signal due to the time jitter:

 $noise(t) = A\omega_{Mod}\Delta t(t)$

If the information would be only on one of the phase of the photodiode signal, the phase noise would not have an impact on our signal at first order. However, there are beams, like B4 on which we are using both phases and therefore the phase noise becomes a problem. Therefore in this note, we will assume that the in-phase and out-of-phase signals have the same amplitude to derive requirements.

The spectrum of a clock phase noise, PN(f), see the figure below as an example, corresponding to the test demodulation board, is usually given as phase variation ($\Delta \omega_{ADC}$) relative to the carrier ω_{ADC} (dBc):

$$PN(f) = \Delta \omega_{ADC}(f) / \omega_{ADC} = \Delta f_{ADC}(f) / f_{ADC}$$

To convert it to a time jitter, one has to divide it by the frequency of the clock.
$$\Delta t(f) = PN(f) / f_{ADC}$$

Therefore:

$$noise(f) = A\omega_{Mod}PN(f)/f_{ADC}$$

$$noise(f) = A2\pi PN(f)f_{Mod}/f_{ADC}$$
(1)



Figure 1 Expected phase noise for the clock of the test demodulation board. The component used is the LMK0408 jitter cleaner.

3 Phase noise measurements with the demodulation test board

The note VIR-0476A-12 described the measurement made with the demodulation test board. The results were the demodulated noise spectrum. However, since the demodulation gives the in-phase and out-of-phase signals it is possible to convert these two signals to a phase and amplitude noises.

Figure 2 presents the result of computation in the case of the 10MHz measurements with the ISLA214 ADC (left plot of figure 8 of VIR-0476A-12). The observed noises are of course due to the signal generators noise plus the ADC noise.

The expected phase noise due to the ADC clock jitter has been added (green curve) on the plot of the phase noise (the left plot of Figure 2). Its trend corresponds to the measured phase noise, validating the order of magnitude of the observed noise.



Figure 2 Phase noise and amplitude noise for the 10MHz signals acquired with the ISLA214 ADC. The plateau of the phase noise above 100Hz is due to the ADC noise floor.

4 Phase noise projections on the tests results (8MHz data)

In this section we present the projection of the expected phase noise on the results of the tests made on the prototype demodulation board presented in VIR-0476A-12. We are using here the 8MHz data for the expected science mode case and loud injections line case (figure 25 of VIR-0476A-12).

The phase noise is computed using the last formula of the section 2. It corresponds to the case of the clock used by the prototype demodulation board and presented in Figure 1 and for 8MHz signals. At 10Hz, the expected phase noise is -71.4 dBc. The amplitude of the science mode 8MHz demodulated signal is 2.3 mV (4.6mV_{pp}). Since the ADC was running at 400MHz, the expected noise, according to the formula (1), is:

Amplitude_noise(10Hz) = $0.0023 \times 2\pi \times 10^{-71.4/20} \text{ 8/400} = 7.8 \ 10^{-8} \text{ V/sqrt(Hz)}$

This is presented in the following figure. There is a good agreement around 10Hz with the signal obtained without phase correction. One can see that the phase noise, especially in the case of the loud injections, is a limiting factor.



Figure 3 Noise of the 8MHz expected demodulated signal for the control signal in science mode (left) and when doing some loud line injections (right). The projection of the ADC clock phase noise (green) has been added.

5 Specifications on the phase noise

The previous section has demonstrated that the phase noise model is valid and applies to our test board. In this section we do the reverse path, namely derive the specifications on the phase noise.

From formula (1), we can see that the coupling of the phase increase with the modulation frequency

There are two different cases, given the expected amplitude of the demodulated signals presented in the table in section 6.1 of VIR-0476A-12.

5.1 Low frequency requirement

This requirement is coming from the demodulation signals. The highest frequency for which we want shot noise limited signals is the 56.4MHz side band. In science mode, the amplitude and the line is 2.3mV (4.6mV_{pp}). A safe requirement is to ask the phase noise to be a factor 10 below shot noise (54 nV/sqrt(Hz)). Therefore, using formula (1) we can derive that the phase noise must be below:

 $20*\log_{10}[54.10^{-9}/(10*2\pi*2.3\ 10^{-3})\ (400/56)] = -111\ dBc$

Notice that taking a factor 10 safety margin, is equivalent to ask that even in the case of loud lines injections, the phase noise is just below shot noise.

5.2 High frequency requirement

Any loud modulation line might coupled to another demodulation line located a few MHz away with the same mechanism. Here we have to considered the loudest lines, the $2f_2$ (113Hz) which has an expected amplitude of 332 mV_{pp} (or A=166mV). Then asking again that the phase noise be a factor 10 below shot noise, we can derive the following limit above 1MHz:

 $20*\log_{10}(54.\ 10^{-9}/(10*\ 2\pi*0.166)\ (400/113)) = -155\ dBc$

6 Summary

This note gives the following requirements for the phase noise of the demodulation ADC clock for the most sensitive photodiode:

phase noise < -111 dBc above 10Hz and -155 dBc above 1 MHz.

Actually, since one of the channels could be used to measure the phase noise, these are the requirements between demodulation ADC of the same DAQ box or for the same group of DAQ boxes used for the same bench.

To compute these requirements, the use of the 2f technique was not considered. This is a way to relax these requirements as it has been demonstrated in VIR-0476A-12.