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First tests of the DAC1955 mezzanine (version 1) for AdV DAQ-Box

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Contents

1 Introduction

The so-called DAQ-Box [1, 2] is being designed to host up to four mezzanines of different types, in particular a DAC mezzanine. The DAQ-Box mother board contains the common interfaces, i.e. a TOLM interface for the timing and data distribution, and an Ethernet link for board management.

General purpose DAC channels will be used in AdV, in particular for the control of the multiSAS suspensions, the OMC, the galvanometers, the locking auxiliary system, the thermal compensation system, the photon calibrator and for noise hunting.

Four prototypes of the DAC mezzanine have been produced end 2012. In 2012, a few test-boards of DAQ-Box have been produced to host one mezzanine. The results of the tests are summarized in this note. DAC outputs have been measured through an ADC channel whose noise may limit the measurements. Different ADC channels have been used in some cases to disantangle sources of noise.

2 The DAC mezzanine

A DAC mezzanine has 8 DAC channel outputs. The digital data sent via the TOLM network are processed via the mother board FPGA[1] associated to the mezzanine, sent to the mezzanine where they are converted by the DAC. The analog signal is low-pass filtered and sent-out as a differential signal via a 3-pin LEMO connector.

The selected DAC chip is AD1955 from Analog Devices. It is a 400 kHz, 24-bit DAC. The following parameters are extracted from the data-sheet [3]:

- SNR: 123 dB,
- Total harmonic distortion: -110 dB,
- Dynamic range: 123 dB.

The output analog anti-image filter is a 2nd order Butterworth filter with cut-off frequency at 60 kHz.

The prototype of the DAC mezzanine has a diffential output with a dynamic range of ±20 V and $\sim \pm 20\,\text{mA}$ maximum current output, with low output impedance (output of an operational amplifier) and no minimum load. The output amplificator is an AD8676. The connector is a 3-pin LEMO.
For channels 00 and 02, the analog output electronics has been modified to add a gain of 0.5: for these two channels, the dynamic range is reduced to ±10 V.

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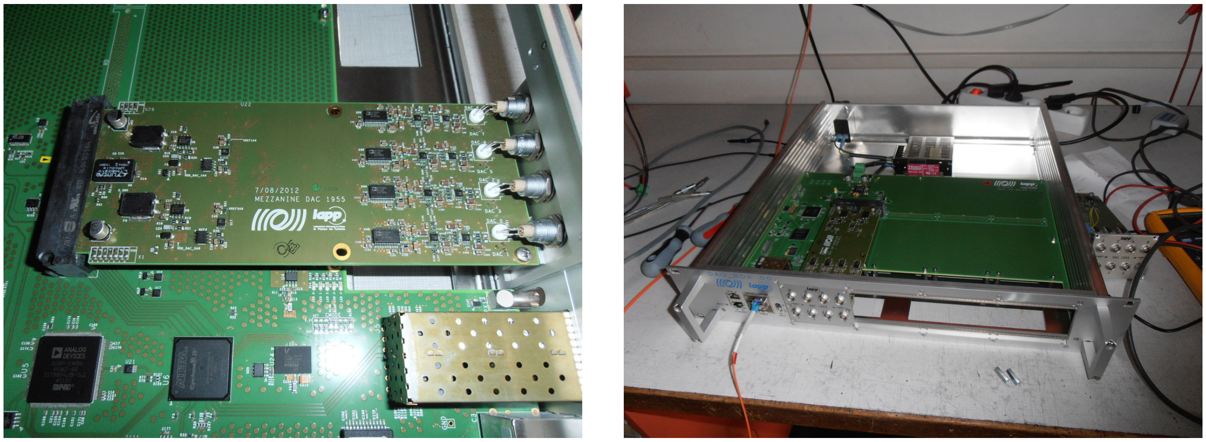
[1] The DSPs have not been used with the firmware version used for these tests.

Pictures of the DAC mezzanine prototype in the DAQ-box test-board are shown if figure 1. Electronics drawings are given in appendix B and in the attached annex file to this document in the TDS [7].



(a) DAC mezzanine prototype.

(b) DAQ-Box test board with the DAC mezzanine.

Figure 1: Picutres of the DAC mezzanine prototype inside the DAQ-Box test-board.

3 Measurements and results

For the tests described in this section, different signals generated on a real-time PC were sent through a TOLM link to the DAQ-box test-board. The data were generated and sent to the DAC chip at 100 kHz. They were extended up to 400 kHz internally, using an option of the DAC chip.

The output analog signal has been measured through an ADC channel from an ADC7674 board [4] with a so-called *flat mezzanine* input, i.e. without analog shaping filter before the ADC and with ±20 V input dynamic.
In some cases, different ADC7674 channels have been used and/or channels from the prototype of the ADC2378 mezzanine, with another ADC chip (LTC2378) [5].

The offsets and gains applied to the generated signals have been calibrated such that the DAC output matches the Pr generated signal. The offsets were of the order of 10 mV and the gains[2] were 1 within better than 1%.

The sign of the DAC output has been checked: for a given generated DC signal, the different DAC outputs have been measured one after the other through the same ADC channel. All the measurements had the same correct sign.

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[2] For the channels with ±10 V dynamic, the gains were of the order of 2.3 V. The "0.5 gain" added in the analog part must be in fact closer to 0.43.

The noise floor of the measurements is first shown. Then, the responses of the DAC to different input signals are measured. Spectrum have been computed with 10 s long FFTs.

3.1 DAC noise floor

The noise floor of the setup, ADC7674 and DAC channel, has been measured sending 0 permanently to the DAC. It is shown in figure 2. The noise floor of the ADC7674 channel used to readout the DAC output is also shown in figure 2.

Above 1 kHz, the measurement is limited by the ADC noise but slightly above it. The noise of the DAC1955 is thus of the order of 200 nV/$\sqrt{\text{Hz}}$ for a dynamical range of ±20 V.

Below 1 kHz, the noise floor is dominated by the DAC noise.

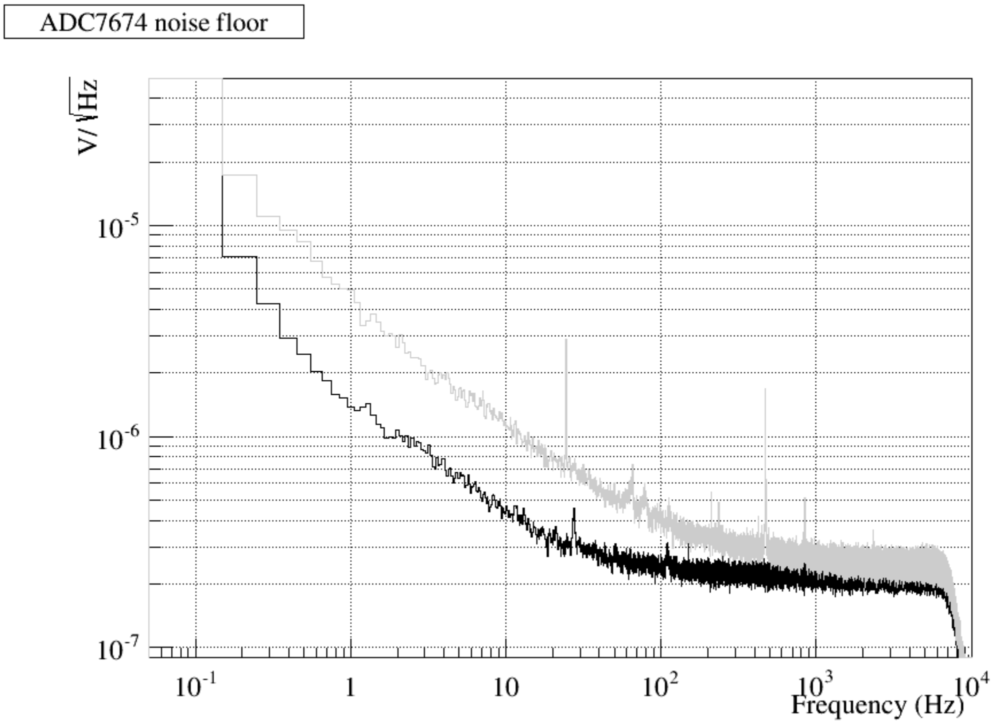

Figure 2: Noise floor. Black: noise floor of the ADC7674 channel (without any input signal). Gray: noise floor of the DAC1955 output readout in a ADC7674 channel.

3.2 Response to sine-wave input and harmonics level

Four different sine-waves of amplitude 1 V have been converted one by one by a DAC channel. The measured DAC outputs are shown in figure 3. For reference, the setup noise floor of the measurement, with 0 V DC input, is drawn. The frequencies of the injected sine-waves are 3.33 Hz, 33.3 Hz, 330 Hz and 3130 Hz.

The presence of harmonics and non-linear noise has been checked, but the DAC or ADC origin cannot be decoupled: they are a factor 10^5 lower than the main line (-100 dB), which is an upper limit for both the DAC and ADC harmonics levels.

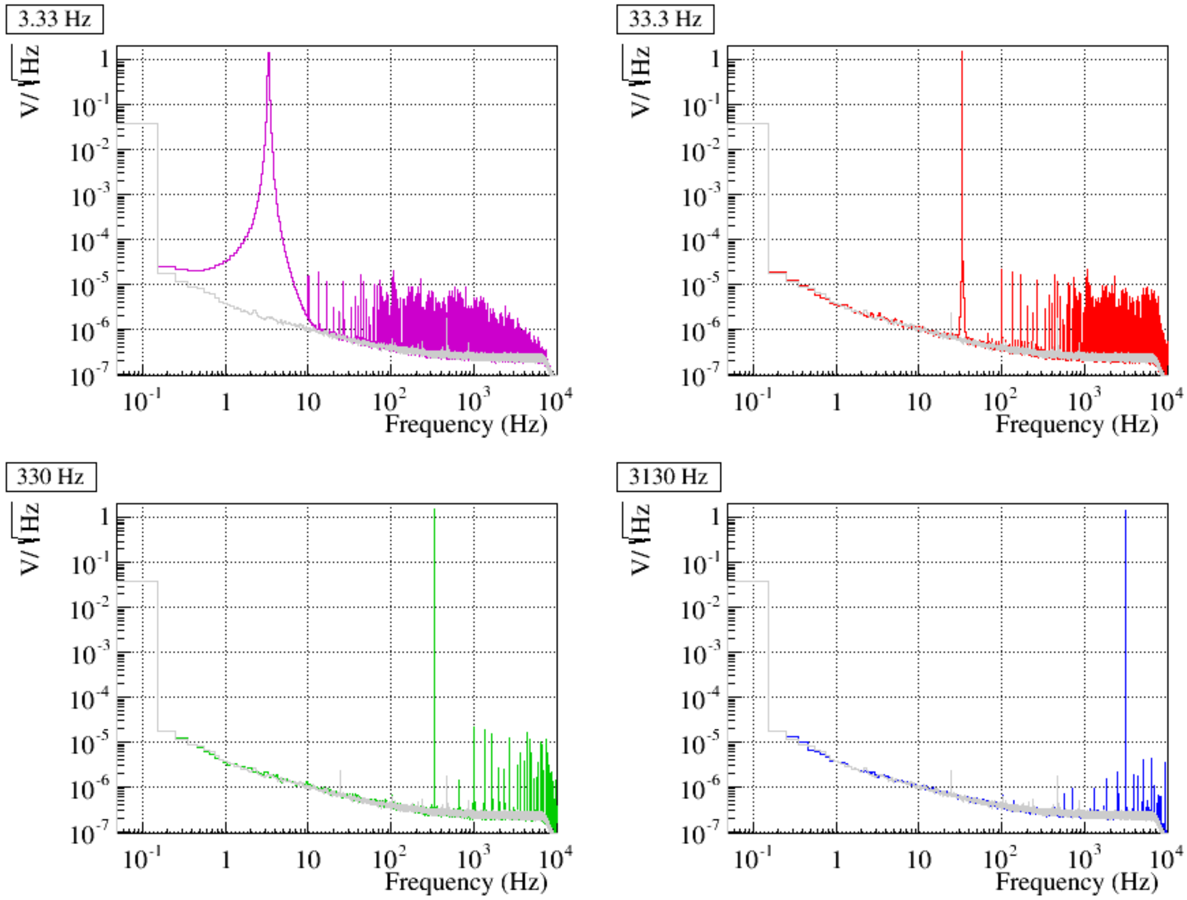

Figure 3: DAC signal with 1 V amplitude sine-wave input. Gray: noise floor (0 V input). Purple:3.33 Hz. Red: 33.3 Hz. Green: 330 Hz. Blue: 3130 Hz.

3.3 Response to DC input

Six different DC inputs have been converted by a DAC channel, from 1 mV to 10 V. The measured DAC outputs are shown in figure 4(a). The setup noise floor of the measurement, with 0 V DC input, is also drawn. The noise above 1 kHz is still limited by the ADC7674 noise.

In presence of a DC input, the output floor noise is increased at low frequency, below few hertz. The increase is less than a factor 2 for DC levels below 100 mV, but more for higher DC levels. In the case of a 10 V DC input, extra-noise is present up to 8 Hz, its level reaching 1 $\mathrm{mV}/\sqrt{\mathrm{Hz}}$ below 20 mHz.

A dithering sine-wave of 1 V amplitude at 3130 Hz was added to the DC input, but had no effect on this low frequency noise.

When splitting the DAC output towards two different ADC channels, both signals are coherent at low frequency. It shows that this noise does not come from the ADC channel.

The figure 4(b) shows the measured DAC outputs for three different DAC channels with DC levels of 1 V and 10 V, as well as the coherence between the channels. The low frequency noise is not coherent between the channels: it highlights that the noise does not come from a common source, such as the power supplies of the mezzanine. The noise levels are slightly different between the channels: it indicates that the noise may come from the DAC1955 chip itself or from its analog output stage.

3.3.1 Miscellanous additionnal tests

Looking for the source of the low frequency noise, different tests have been done:

- stop the transmission of the data to the DAC[3]: the DAC continues to generate the last value it has received.
- idem, and also stop the clock[4] MCLK. The DAC continues to generate the last value it has received.
- add the timing synchronization of the DAQ-Box DC/DC module at 500 kHz.
- add the timing synchronization of the DC/DC convertor of the mezzanine, with synchronization frequency of 1 MHz.

None of these modifications and tests have had impact on the noise level.

Other measurements were done generating a DC signal and a line at 1117 Hz. The measured signals have then been digitally demodulated at 1117 Hz (using Pr) in a real-time PC. As expected, the amplitude of the demodulated signal and the DC signals are coherent, and have the same level when the amplitude of the line is the same of the DC value. It confirms that the low frequency noise is picked-up by the DC signal of the line proportionnally to their level.

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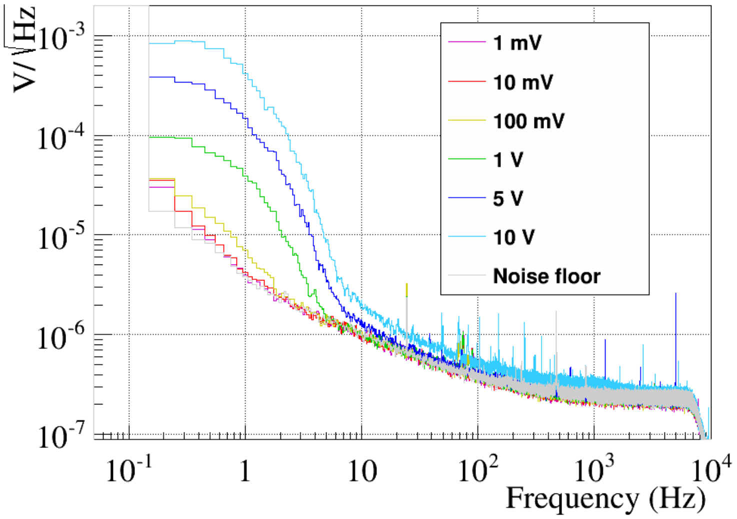
[3] LRCLK, SDATA, BCLK

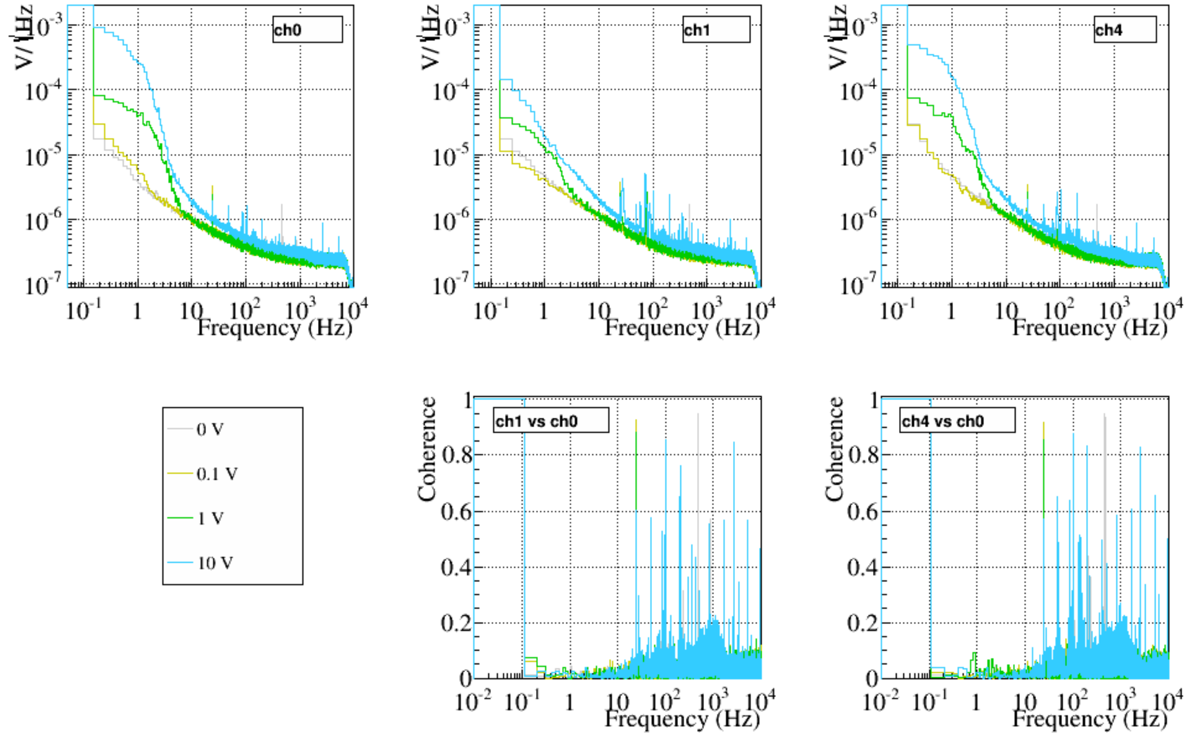
[4] MCLK

3.3.2 Comparison of channels with different output dynamics

The comparison of the channels 01 and 03 (±20 V dynamics) with the channels 00 and 02 (±10 V dynamics) is shown in figure 5. A trend seems to indicate that the channels with reduced dynamic has slightly lower noise (by $\sim 20\%$) at frequences higher than few tenth of hertz, and have larger noise at low frequencies. However, also channels with the same dynamic have different noise levels, which makes difficult to conclude with only four channels.



(a) DAC signal with DC inputs. Gray: 0 V. Purple: 1 mV. Red: 10 mV. Yellow: 100 mV. Green: 1 V. Blue: 5 V. Cyan: 10 V.



(b) Outputs of 3 different DAC channels with DC inputs, readout by 3 different ADC7674 channels. Top: 3 DAC outputs; gray: noise floor; yellow: 0.1 V DC; green: 1 V DC ; cyan: 10 V DC. Bottom: coherence between the DAC channels (left: ch1 and ch0; right: ch4 and ch0).

Figure 4: Measurements with DC inputs.

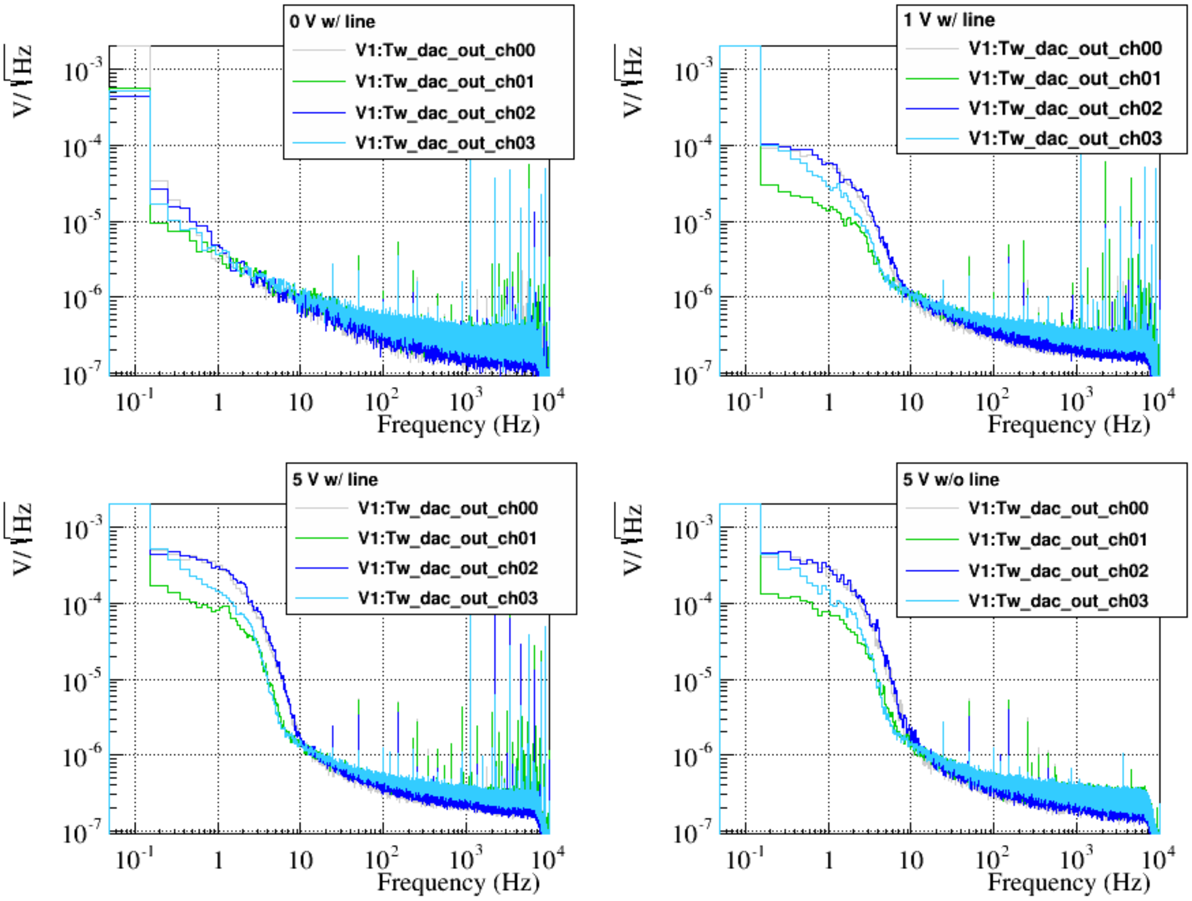


Figure 5: Comparison of 4 DAC channels with some DC levels.

3.4 Response to low-frequency band-limited input

Typical control signals in Virgo have components at low frequency only and a sharp cut-off at few hertz of tens of hertz. In order to check the response of the DAC channels to this type of signals, white noise has been generated and low-pass filtered with a 8th order Butterworth filter before being sent as input signal to the DAC channel. Different levels of white noise and cut-off frequencies have been applied (see appendix A).

The measured DAC output is shown in figure 6 in the case of a noise signal with amplitude 1 $\mathrm{V}/\sqrt{\mathrm{Hz}}$ up to 1 Hz. Some non-linear noise appears after the sharp edge of the input signal, between few hertz and 1 kHz. In order to understand the origin of this noise, DAC or ADC channel, the DAC output has been sent to two different ADC channels[5]. The noise disappears in presence of a high frequency dithering sine-wave (1 V amplitude at 3130 Hz) added to the DAC input signal. In presence of the non-linear noise, the coherence between the signals from the two ADCs is very low in the range 5 Hz to 1 kHz. This indicates that the noise comes mainly from the ADC channel and not from the DAC channel.

To conclude, the red curve of the second plot (measured with LTC2378 chip) is an upper-limit on the non-linear noise induced by the DAC channel when the input is a band-pass signal with cut-off frequency around 1 Hz.

4 Conclusion

Four prototypes of DAC1955 mezzanines have been produced and validated at LAPP [6]. The noise floor, the harmonics level in the case of generation of sine-wave signals and the non-linear noise in the case of typical Virgo signal dominated by the low frequency components have been estimated. The presence of some extra-noise present at low frequency in the case of the generation of a DC analog signal has been shown in section 3.3.

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[5] One is the standard ADC7674 channel, the other one is a channel with a LTC2378 chip, selected for the ADC mezzanines of the DAQ-Box [5].

[6] One DAC1955 mezzanine is being used succesfully to lock the AdV OMC on the LAPP test-bench [8].

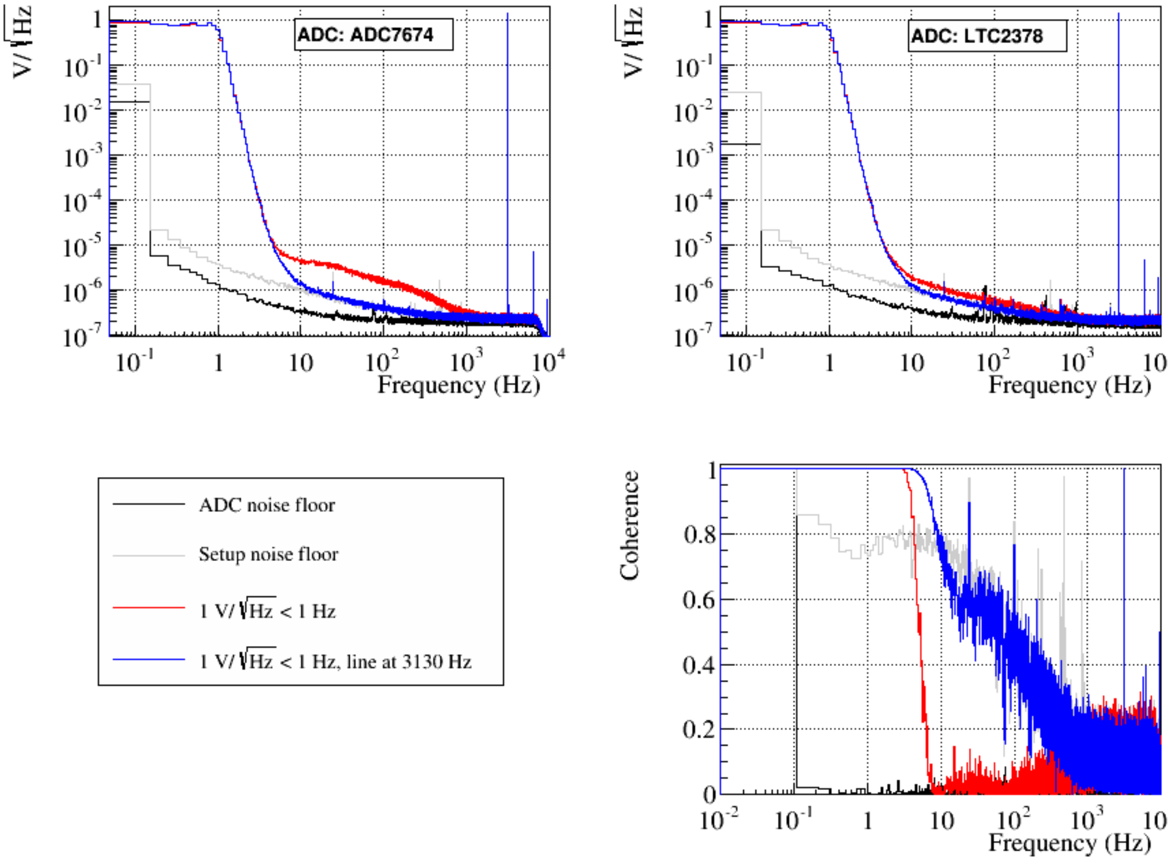


Figure 6: Top: DAC channel output measured through two ADC channels. for a band-limited input and eventually a high frequency line. Bottom: coherence between the same DAC signal but measured by the two different ADC channels. Black: ADC noise floor (no ADC input). Gray: setup noise floor (0 V DC DAC input). Red: band-limited input, $1\ \mathrm{V}/\sqrt{\mathrm{Hz}}$ *up to 1 Hz. Blue: same band-limited input with a 1 V amplitude line at 3130 Hz.*

References

[1] The Virgo collaboration, VIR-0128A-12 (2012), *Advanced Virgo Technical Design Report*

[2] N. Letendre at al., Virgo note VIR-0108A-12 (2011), *Preliminary DaqBox Specifications*

[3] Analog Devices, AD1955 datasheet

[4] N. Letendre et al., Virgo note VIR-0109A-12 (2012) *ADC7674 user manual*

[5] T. Bouedo et al., Virgo note VIR-0122A-13 (2013) *Tests of the ADC to be used by the DAQ Box*

[6] L. Rolland, Virgo presentation VIR-0369A-13 (2013) *DAQ sub-system status*

[7] Annex file attached to the note VIR-0170A-14

[8] R. Bonnand et al., LVC meeting VIR-0093A-14 *Advanced Virgo OMC test*

A Response to low-frequency band-limited inputs

Measurements are described in section 3.4. The non-linear noise seen in the measurements is dominated by the non-linear noise from the ADC7674 channel.

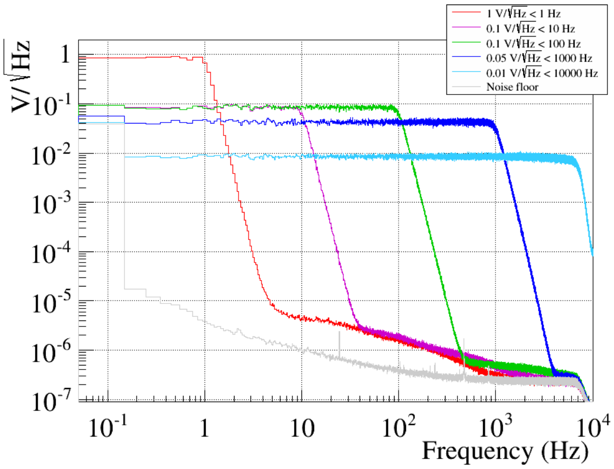
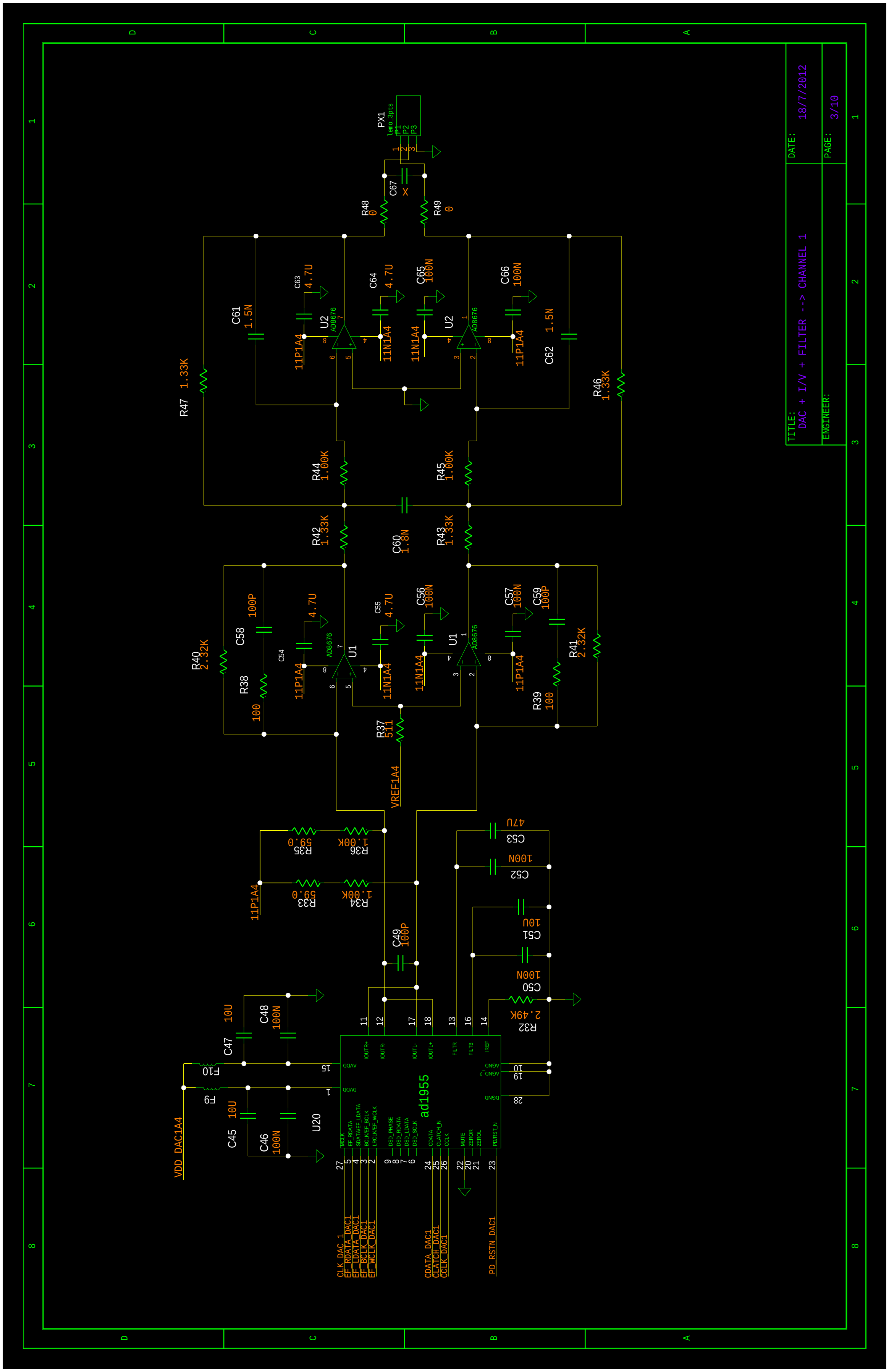


Figure 7: DAC channel output for different band-limited noises. Red: noise floor (0 V input). Black: $1\ \mathrm{V}/\sqrt{\mathrm{Hz}}$ *up to 1 Hz. Purple:* $0.1\ \mathrm{V}/\sqrt{\mathrm{Hz}}$ *up to 10 Hz. Blue:* $0.1\ \mathrm{V}/\sqrt{\mathrm{Hz}}$ *up to 100 Hz. Cyan:* $0.05\ \mathrm{V}/\sqrt{\mathrm{Hz}}$ *up to 1 kHz. Green:* $0.05\ \mathrm{V}/\sqrt{\mathrm{Hz}}$ *up to 10 kHz.*

B DAC mezzanine drawings

The electronics drawings of the DAC mezzanine are reported in the file joint to this document in the TDS [7]. Extracted from this document, the drawing of a channel with the DAC chip, the current to voltage converter and the output analog filter is reported in the next page.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DATE: 18/7/2012
PAGE: 3/10
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ad1955
VDD_DAC1A4
F9
F10
C45 10U
C46 100N
C47 10U
C48 100N
C49 100P
C50 100N
C51 10U
C52 100N
C53 47U
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R33 59.0
R34 1.00K
R35 59.0
R36 1.00K
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R37 511
R38 100
R39 100
R40 2.32K
R41 2.32K
C54 4.7U
C55 4.7U
C56 100N
C57 100N
C58 100P
C59 100P
U1 AD8676
11N1A4
R42 1.33K
R43 1.33K
C60 1.8N
R44 1.00K
R45 1.00K
R46 1.33K
R47 1.33K
C61 1.5N
C62 1.5N
C63 4.7U
C64 4.7U
C65 100N
C66 100N
U2 AD8676
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R49 0
C67 X
PX1 lemo_3pts
P1
P2
P3
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EF_RDATA_DAC1
EF_LDATA_DAC1
EF_BCLK_DAC1
EF_WCLK_DAC1
CDATA_DAC1
CLATCH_DAC1
CCLK_DAC1
PD_RSTN_DAC1
A
B
C
D
1
2
3
4
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6
7
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